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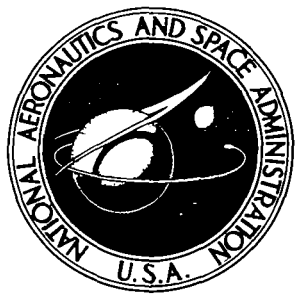

NASA CR-1348

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RELIABILITY HANDBOOK FOR SILICON MONOLITHIC MICROCIRCUITS

Volume 3 — Failure Analysis of Monolithic Microcircuits

by Wilton L. Workman

Prepared by
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas
for George C. Marshall Space Flight Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • APRIL 1969

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Volume 3 - Failure Analysis of Monolithic Microcircuits

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FOREWORD

This handbook was prepared as an aid in determining the most effective application, testing, handling, and quality and reliability assurance controls for integrated circuits. It was compiled in two books of two volumes each and deals primarily with the subjects of application, failure mechanisms, failure analysis, and reliability assessment. Some similarity may be noted between NASA CR 1110, "Microelectronic Device Data Handbook," and the data presented herein; however, NASA CR 1110 deals with microcircuits in general, while this document was prepared as a reliability handbook and deals with monolithic microcircuits only.

The effort resulting in the publication of this handbook was produced under the technical direction of the Parts and Microelectronics Technology Branch, Future Programs and Technology Office, Quality and Reliability Assurance Laboratory, George C. Marshall Space Flight Center, Alabama.

D. Grau
Director, Quality and Reliability
Assurance Laboratory

PREFACE

This publication, "Failure Analysis of Monolithic Microcircuits," is Volume 3 of a four-volume series entitled, "Reliability Handbook for Silicon Monolithic Microcircuits." The Handbook was prepared for the National Aeronautics and Space Administration by Texas Instruments Incorporated, under Contract NAS 8-20639. The Handbook series consists of the following volumes:

Volume 1	Application of Monolithic Microcircuits
Volume 2	Failure Mechanisms of Monolithic Microcircuits
Volume 3	Failure Analysis of Monolithic Microcircuits
Volume 4	Reliability Assessment of Monolithic Microcircuits

The purpose of the Handbook is to provide aid in determining the most effective application and understanding of monolithic microcircuits, and the most effective quality and reliability assurance controls for the circuits.

Volume 3, "Failure Analysis of Monolithic Microcircuits," describes:

- Effective failure analysis methods.
- A step-by-step procedure for performing failure analysis.
- How to identify failure mechanisms and their causes.
- How to assess the results of a failure analysis and to establish a relationship between the findings and the affected parameters or characteristics.

Acknowledgement is made of Buehler, Ltd. and Adolph I. Buehler, Inc.'s permission to include certain of their data on materials and techniques used in rough polishing a metallurgical microsection of a semiconductor element.

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VOLUME 3

FAILURE ANALYSIS OF MONOLITHIC MICROCIRCUITS

SECTION I

INTRODUCTION

Failure Analysis may be defined as the process of determining why a device has malfunctioned or failed to meet established requirements. The scope of this process may range over the broad area between device defects and improper application or test. The objective of this Volume 3 of the Handbook is to present a sequence of methods which will enable a failure analyst to perform successful failure analysis on semiconductor microcircuits.

Several requirements must be met for a failure analysis process to be fully successful. First, some information concerning the initial rejection is preferable. This information should consist of detailed conditions existing at the time of failure, such as failed parameter readings, circuit application, environmental factors, etc. Second, a collection of facts revealing the present condition of the device must be made. These facts may relate to mechanical, electrical, chemical or other characteristics. Third, a comparison of the information obtained in the first two steps is required. Some correlation must exist between the present condition and the rejection reason in order to draw concrete conclusions.

The procedure for collecting the factual information representing the present condition of the device must be planned to obtain maximum information. A procedure which has been used successfully many times is as follows:

1) Review available failure information
2) Radiographic analysis
3) Hermeticity analysis
4) Preliminary electrical tests:
    a) Threshold
    b) Isolation
    c) Pin-to-pin
    d) Parameter

5) Decap

6) Visual microscopic inspection

7) Electrical probe, if necessary and/or element isolation

8) Metalization removal and/or microsection, if necessary

Items 2, 3 and 4 may be performed in any sequence with little danger of losing useful information.

This Volume presents each aspect of the failure analysis process in detail, although not necessarily in the order of most beneficial performance. The individual situation frequently will dictate a specific sequence.

SECTION II

EVALUATION OF THE MONOLITHIC MICROCIRCUIT PRIOR TO OPENING THE PACKAGE

A. REVIEW OF AVAILABLE FAILURE INFORMATION

Prior to opening the monolithic microcircuit's package, all possible information must be obtained concerning the behavior of the failed device. The first step in gaining this information is a complete review of the available failure information at the time the microcircuit is received for analysis. The information received may range from the very vague to the complete information furnished by parameter measurements. For instance, the fact that the microcircuit caused a system failure is of little value in assisting the analyst to make a preliminary diagnosis of the failure mode involved. On the other hand, failure information such as inability of the device to change states, or that it has no output in one section, can simplify the analyst's job by causing him to suspect one specific area of the microcircuit. Care must be exercised to determine that the information received is consistent within itself to prevent erroneous conclusions.

The review of available failure information becomes increasingly important when it cannot be verified that the microcircuit is a failure and the failed condition must be duplicated by the analyst. This review also assists the analyst in separating the true failure mode from apparent failure modes created by improper handling of the device following the observed failure.

Following the review of all available failure information, the microcircuit may then be submitted to electrical tests to verify that the information received is correct.

B. VERIFICATION OF FAILURE INFORMATION

1. General

Parameter measurement is one important step in determining the validity of failure information. Digital device parameters such as input current, "on" voltage level, "off" voltage level and switching times provide a basic measurement of device operating condition. Linear device parameters such as offset voltages, gain and ac signal swing provide the same information for these type devices.

Once parameter values are known, the failure information from the user can be evaluated objectively. Comparison of the parameter data and failure information usually results in good correlation or confirmation that the original failure information is accurate. Occasionally, all parameters test good. The immediate suspicion is that the original failure information is inaccurate. In that case special procedures must be followed to determine if the device failed due to improper application, temperature sensitivity or intermittent conditions. The trouble may even have rectified itself. A visual inspection is required to test this possibility. A detailed discussion of these topics will now be presented.

2. Applicable Parameter Tests, Equipment Required

a. Digital Devices

(1). Resistor-Capacitor-Transistor Logic. Four basic parameters may be used to determine the operating characteristics of resistor-capacitor-transistor logic (RCTL). These basic parameters are as follows:

- Input current
- "On" voltage level
- "Off" voltage level
- Dynamic test

The normal temperature extremes of operation are −55°C to +125°C; therefore, the dc parameter tests are usually made at these extremes to insure proper operation over the entire temperature range.

The input current test is performed by applying a specified voltage to one input pin while applying a specified V_{cc} and ground connection, and grounding all other unused inputs. (Refer to Figure 3-1. The applied input voltage is then dropped across the input resistor and the base-emitter diode of the output transistor. The current is read at the input pin, and acceptable limits are based on a worst-case design tolerance over the temperature range.

The "on" voltage test, shown in Figure 3-2, is designed to determine if the output is capable of supplying the logic "one" condition to the input of another RCTL device. The test is performed in a manner that is similar to the input current test. The exceptions are that the applied input is the specified absolute minimum input which will insure "turn-on" of the output transistor, and the output voltage is monitored rather than the input current.

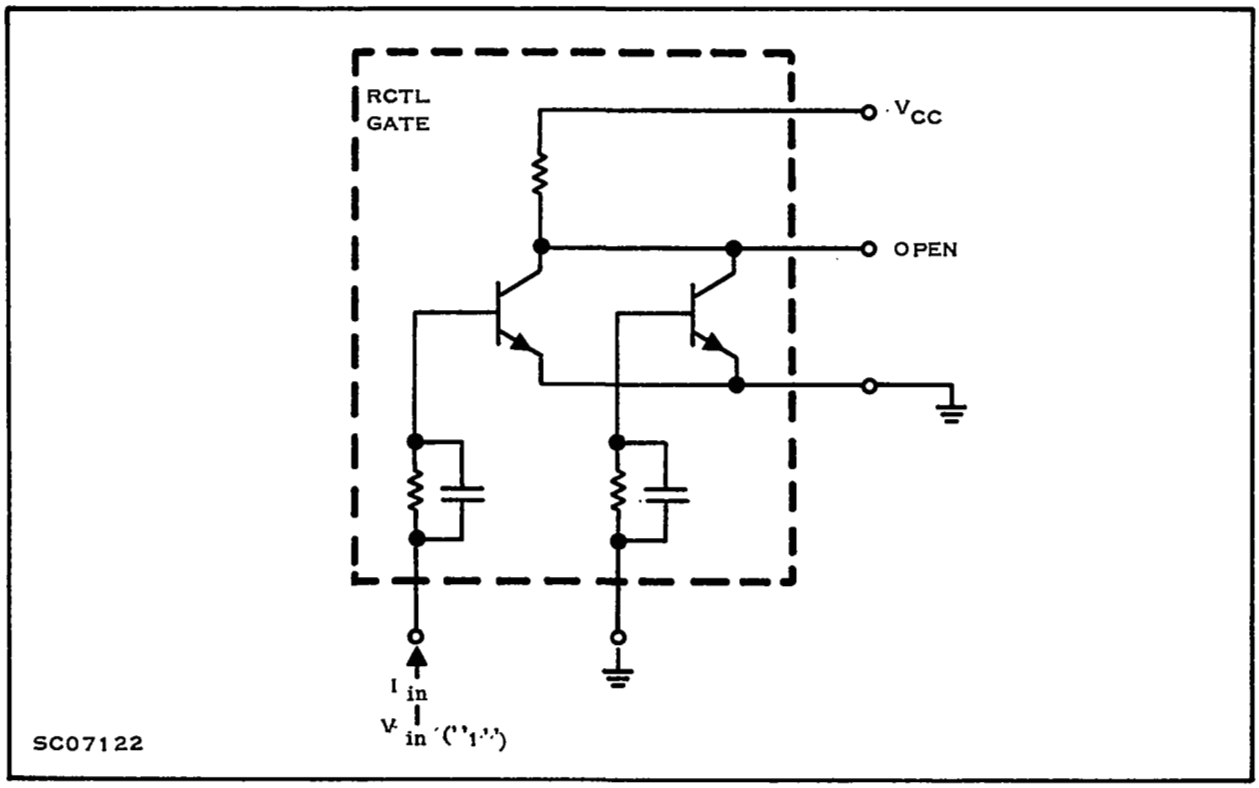

Figure 3-1. Input Current Measurement Circuit for RCTL Device

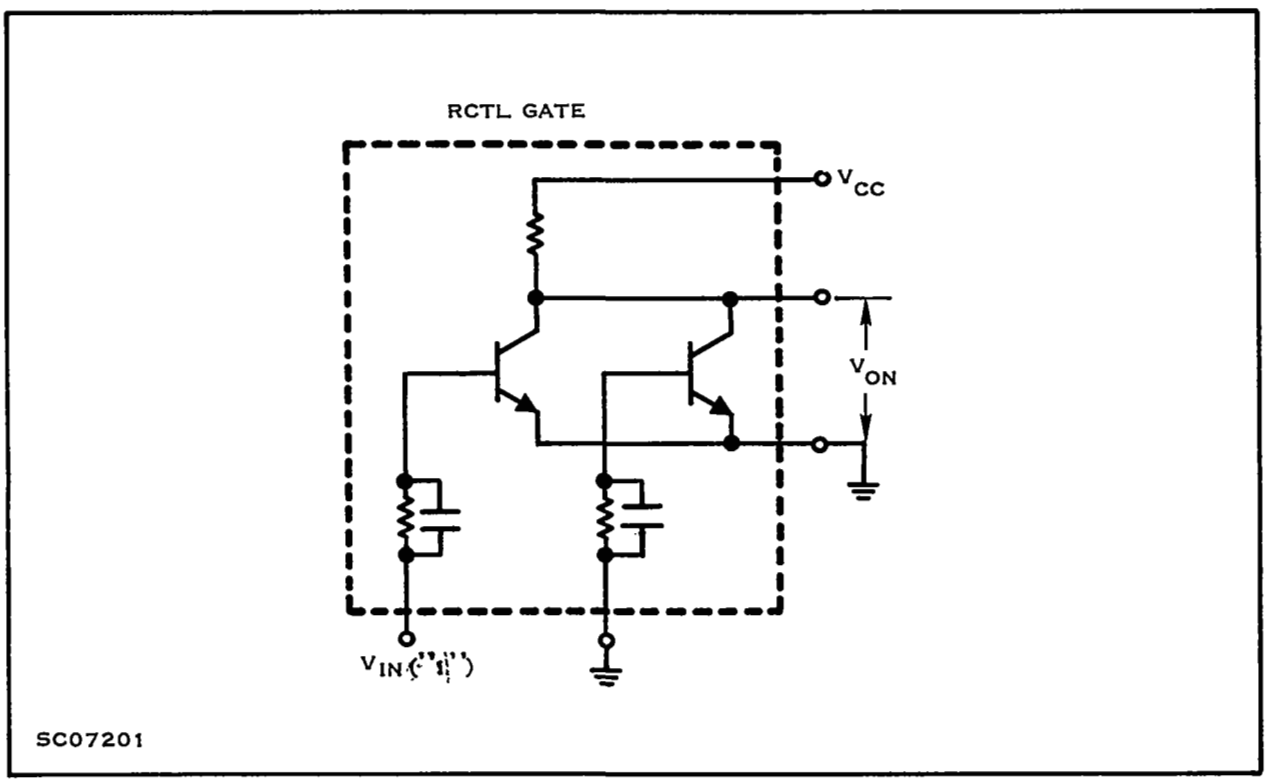

Figure 3-2. "On" Voltage Measurement Circuit for RCTL Device

The "off" output voltage test, shown in Figure 3-3, is designed to determine the logic "zero" level at the output transistor. The logic "zero" output voltage must be of sufficient value to ensure "turn-on" of other gates or logics to which the output may be applied. The device is, therefore, tested with load and without load to determine if the device has the proper or specified output voltage capabilities. The loading of the output is accomplished by applying a resistor and a diode to ground. The value of the resistor is dependent on the number of "n" loads required. The test is performed in a manner similar to that of the "on" voltage test, except that the output is loaded and the applied input voltage is the specified absolute maximum voltage that will insure "turn-off" of the output transistor.

The ac or dynamic test (Figure 3-4) merely determines if the device performs the "on" and "off" voltage-level requirements at a prescribed repetition rate, and whether or not the logic function changes within a specified length of time. The output for this test is loaded with a 20-kΩ resistor that is in series with and connected to the anode of a 1N914 diode across which a capacitor of value C_S is connected. The value of C_S should be selected so that the total capacitance of the test fixtures, connectors, scope probe and C_S is equal to 50 $\mu\mu$F. Unused inputs should be grounded when not in use during the ac test.

The previously described test parameters should be applied to the data sheet or other contractual agreement in such a manner as to assure that the device functioned in accordance with published specifications or that the failure symptoms correlate with the failure parameters observed.

The equipment required for testing the dc parameters of an RCTL device is:

- One voltmeter with a 0-to-10 V capability and a 10-MΩ or higher input impedance.
- One current meter with a 1 μA-to-10 mA current-range capability.
- Three dc power supplies with a voltage range that is variable from zero to 8 V.
- A test fixture and sufficient interconnecting cables to connect power supplies and monitoring meters.
- A resistor and a diode for output loading.

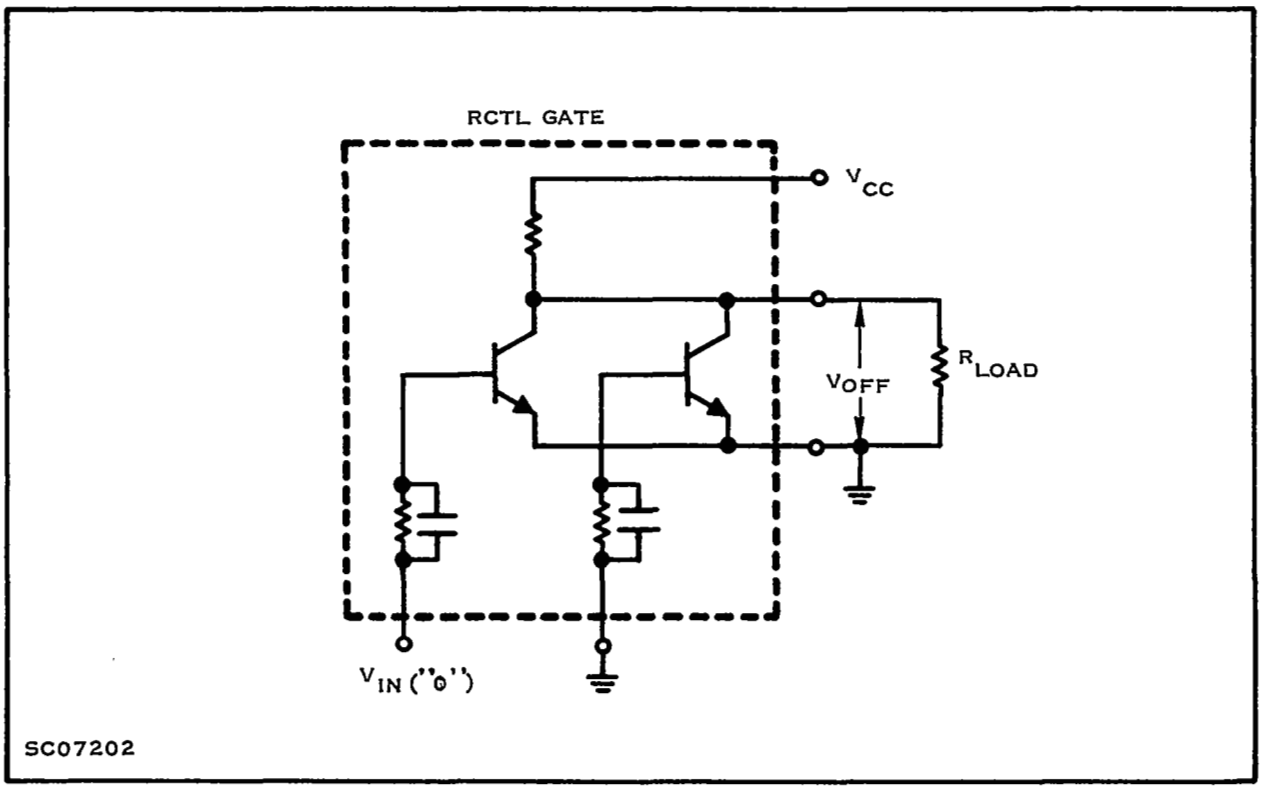

Figure 3-3. "Off" Voltage Measurement Circuit for RCTL Device

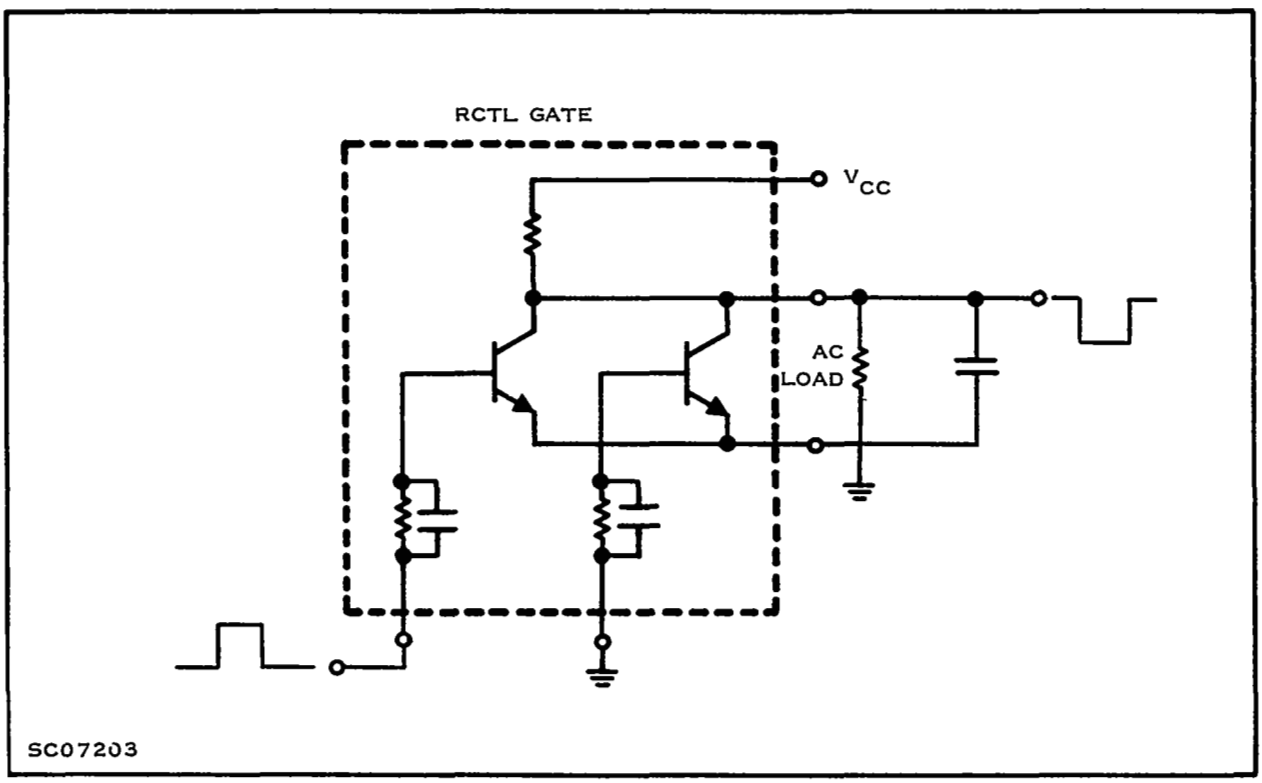

Figure 3-4. Dynamic Test Circuit for RCTL Device

In addition to the equipment listed for the dc tests, the following is required for ac parameter measurements:

- One pulse generator with frequency capabilities up to 1 MHz, pulse amplitudes of 0-to-8 V, and independent rise and fall time capabilities of 15 ns.
- One syncroscope or dual trace oscilloscope with internal rise time characteristics equal to or less than 15 ns, internal impedance of 1 MΩ or greater, and voltage magnitudes of 0.5 V per cm to 2 V per cm.
- A test fixture.
- One 20 kΩ resistor.
- One 1N914 diode.
- One capacitor (C_s)

All of the above equipment may be built into a permanent console arrangement as illustrated in Figure 3-5.

(2). Diode-Transistor Logic. There are six basic parameters that may be used to test the diode-transistor-logic (DTL) devices. These basic parameters are as follows:

- V_{cc} current
- Input current
- Output current
- Input voltage
- Output voltage
- Dynamic test

The temperature extremes of operation may be specified from −55°C to +125°C; therefore, the dc parameter measurements are usually made at these extremes to insure proper operation over the entire temperature range.

The V_{cc} current is measured at two conditions: with the outputs at logical "zero," and with the outputs at logical "one." To measure the V_{cc} current with the outputs at logical "zero," as shown in Figure 3-6, all inputs are either open circuited or reverse biased to insure that the outputs are low, or saturated. With the output pins open circuited, the V_{cc} current is that current required by the bases of the output transistors and the "pull-up" resistors. To measure the V_{cc} current with the

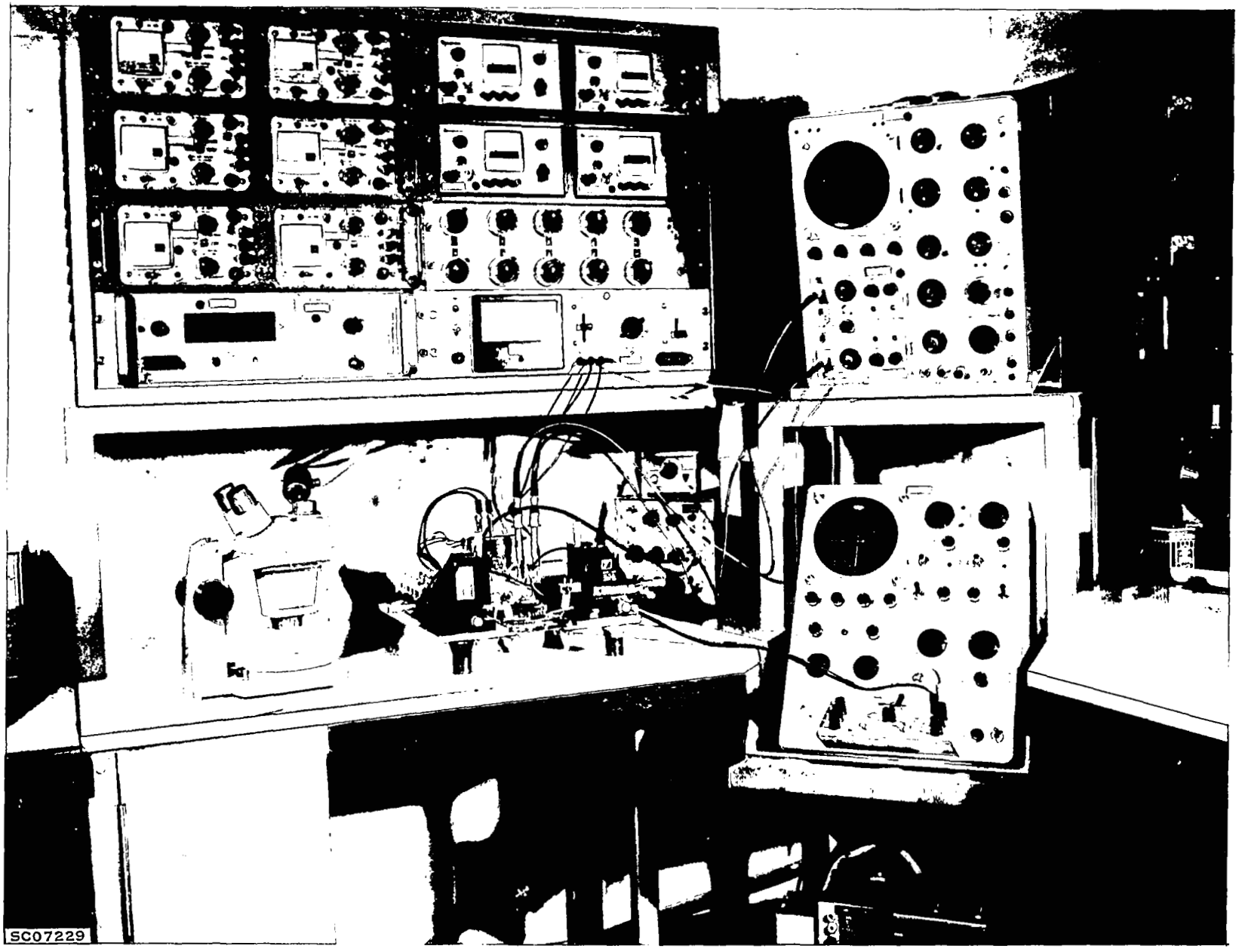

Figure 3-5. Test Console for Monolithic Microcircuit Failure Analysis

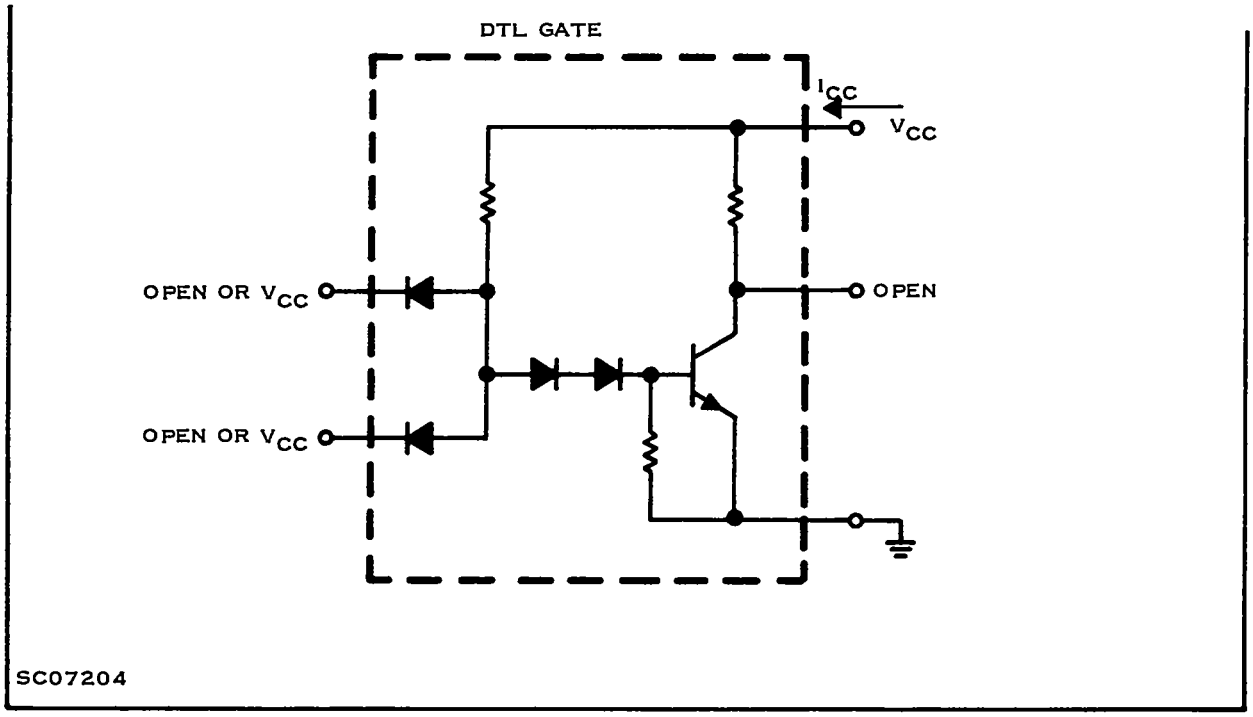

Figure 3-6. "Zero" V_{cc} Current Measurement Circuit for DTL Device

outputs at logical "one" (Figure 3-7), all inputs are open circuited or reverse biased, with the exception of one input for each gate, which is grounded. With the output pins open circuited, the V_{cc} current is the sum of the currents drawn by each grounded input.

The input current is also measured at the logical "zero" condition and at the logical "one" condition. The logical "zero" input current, Figure 3-8, is measured for each input by taking that input to ground through a current meter while all other inputs are open circuited or reverse biased. The logical "zero" input current is then the current drawn through the forward-biased input diode from V_{cc}. The logical "one" input current (Figure 3-9) is essentially the reverse leakage of the input diode. This measurement is obtained for each input by applying a sufficiently high voltage (to insure reverse biasing) through a current meter to that input while all other inputs are open circuited or grounded. If the other inputs are open circuited, the V_{cc} and ground pins are normally grounded. If the other inputs are grounded, the recommended V_{CE} voltage is applied to the V_{cc} pin with respect to the ground pin.

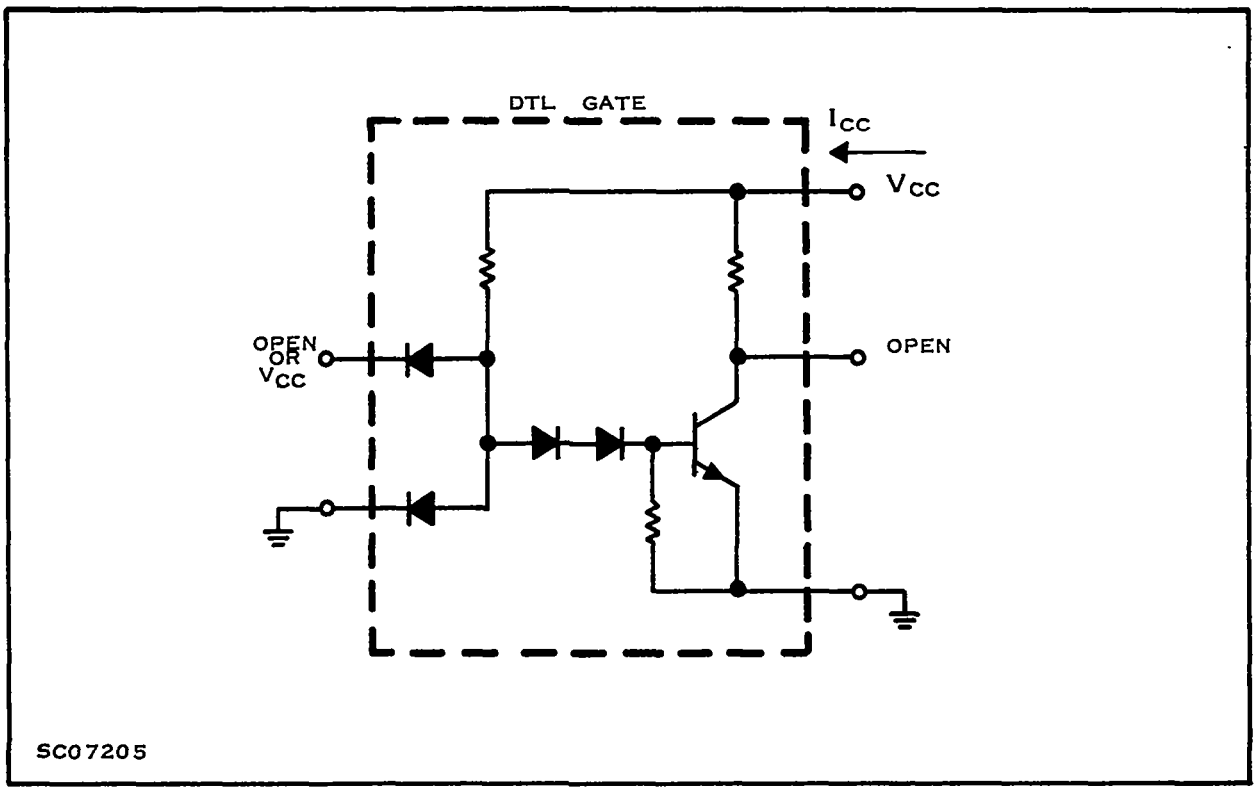

Figure 3-7. "One" V_{CC} Current Measurement Circuit for DTL Device

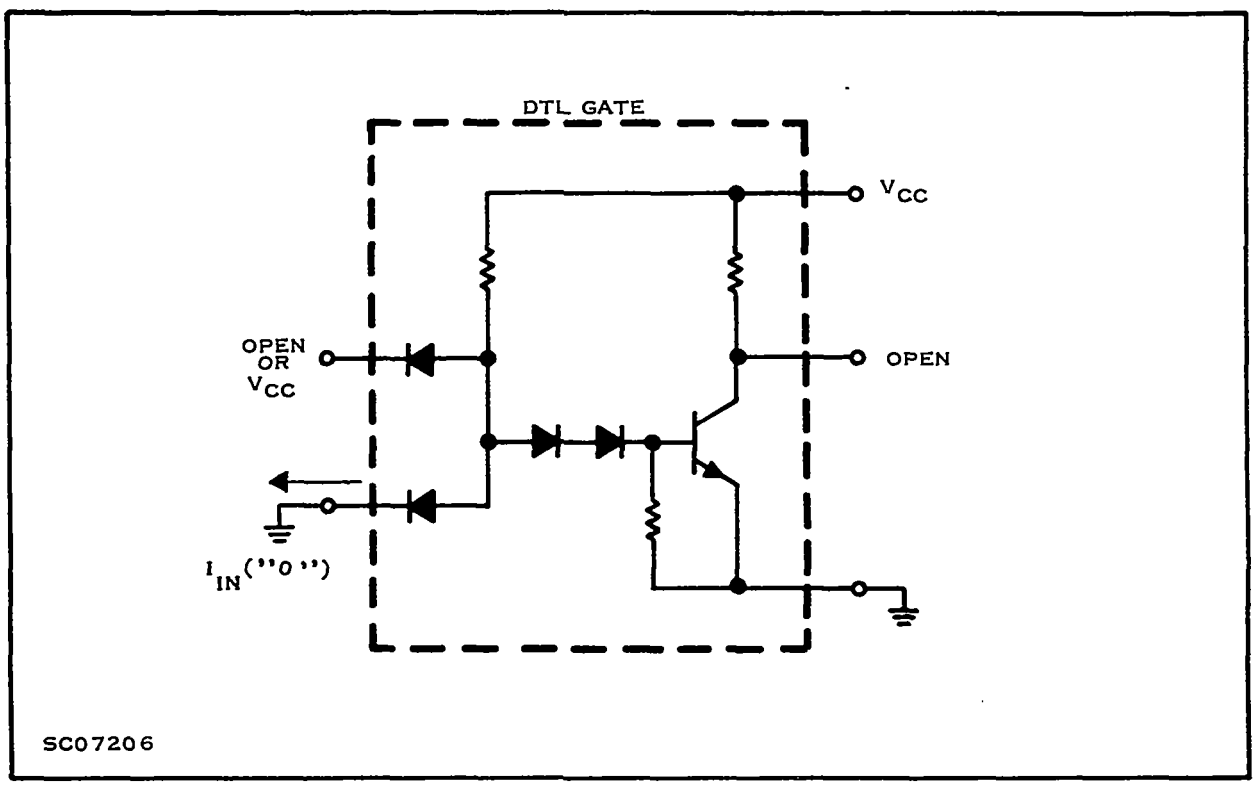

Figure 3-8. "Zero" Input Current Measurement Circuit for DTL Device

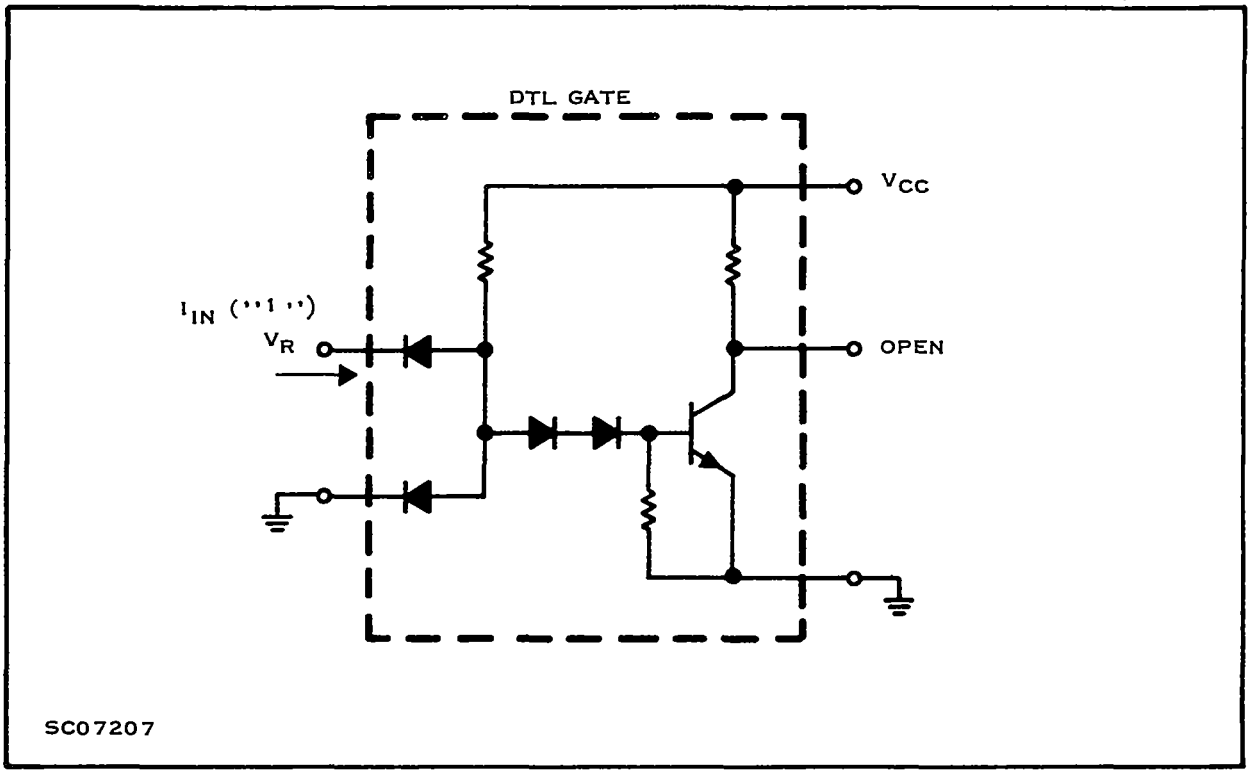

Figure 3-9. "One" Input Current Measurement Circuit for DTL Device

The output currents are usually measured at two conditions: with the output short-circuited, and with the output reverse-biased (logical "one"). The short-circuit output current (Figure 3-10) is obtained for each output by measuring the current through the output pin from V_{cc} when the output is grounded through a current meter. The inputs are taken "low" to insure that the output transistor is biased "off." Thus, the current measured is a function of the current drained through the "pull-up" resistor. The reverse bias output current (logical "one"), as shown in Figure 3-11, essentially tests the reverse bias characteristics of the output transistor. The output pin in this case is normally tied to V_{cc} through a current meter while the inputs are taken "low," either separately or together, to insure a logical "one" condition. The current is thus the reverse leakage of the output transistor.

The input voltage test (Figure 3-12), determines the breakdown characteristics of the input diode. With the V_{cc} pin, the output pin and the ground pin grounded, a positive voltage is applied to each input separately through a current meter. This positive voltage is adjusted to allow 10 μA of current to flow through the input pin. This voltage is called the reverse input voltage or BV_j.

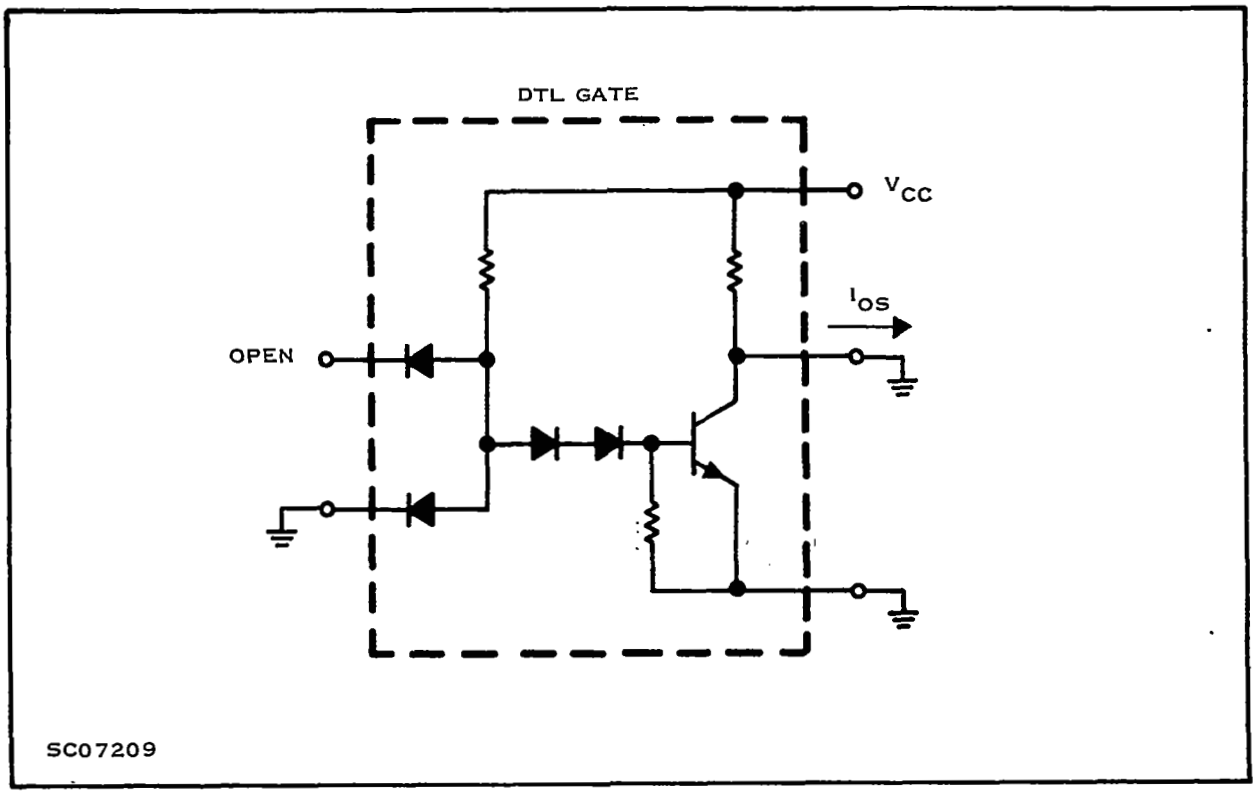

Figure 3-10. Short-Circuit Output Current Measurement Circuit for DTL Device

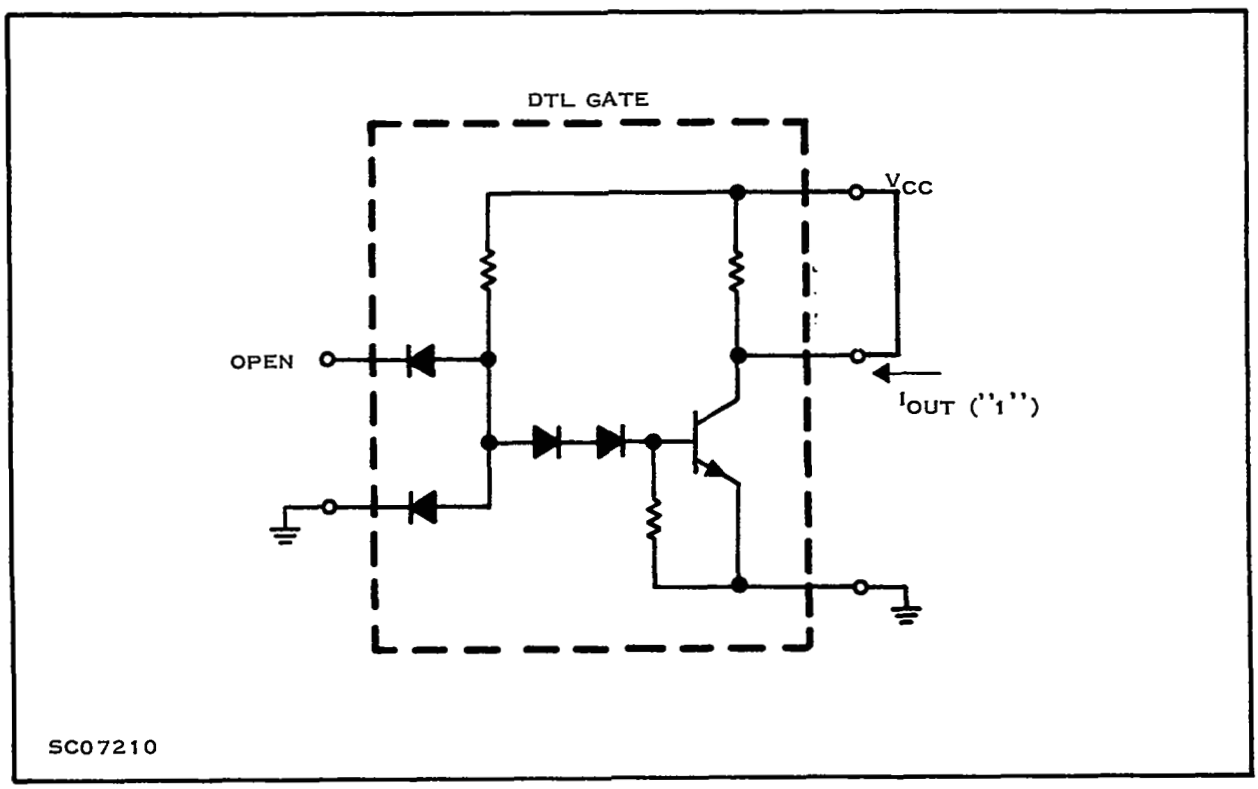

Figure 3-11. Logical "One" Output Current Measurement Circuit for DTL Device

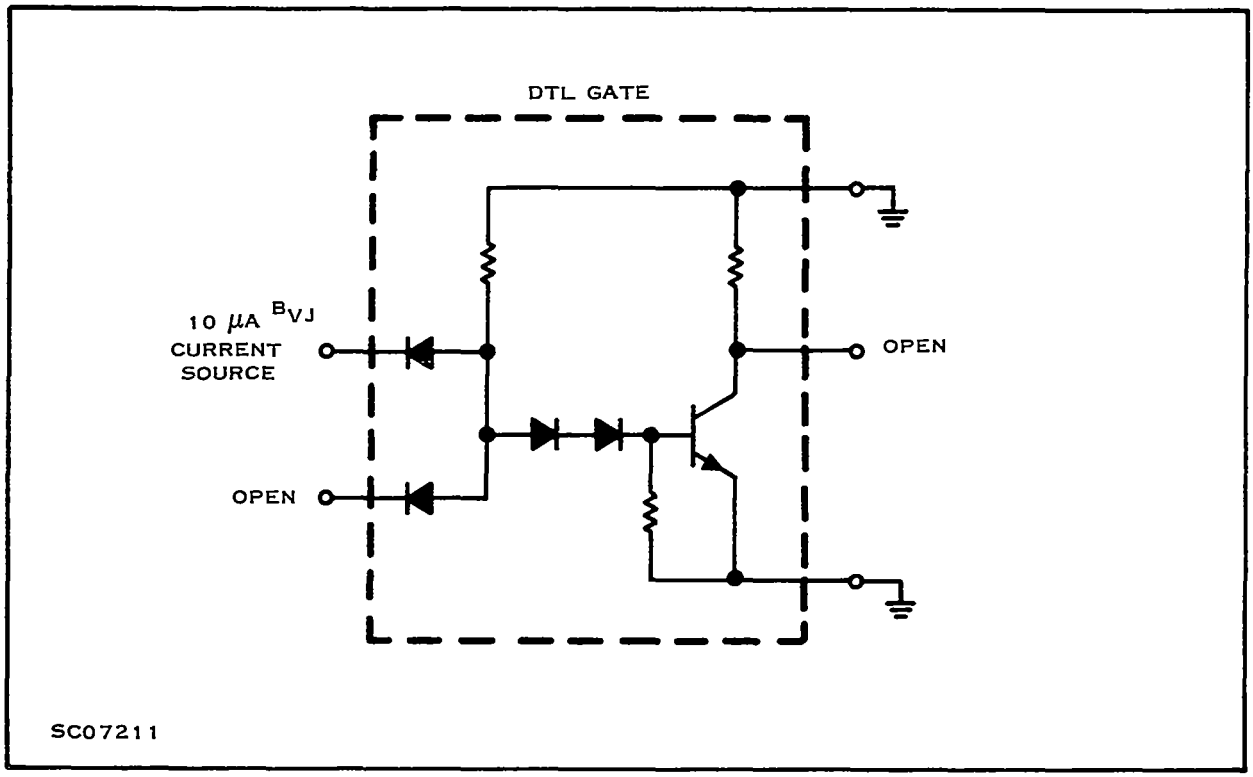

Figure 3-12. Input Voltage Measurement Circuit for DTL Device

The output voltages are measured at the logical "zero" output voltage and the logical "one" output voltage. The logical "zero" output voltage test, Figure 3-13, is performed to determine that the output voltage is "low" (logical "zero") when the minimum logical "one" input voltage is applied. The applied input voltage is the lowest reverse voltage which will turn the output transistor "on," and is applied to one input while the other inputs are open-circuited or tied to V_{cc}. The output receives a sink current which represents the maximum number of logical "zero" inputs that the output is expected to sink. The logical "zero" output voltage is a $V_{CE(sat)}$ characteristic, measured from the output pin to ground. The logical "one" output voltage test, shown in Figure 3-14, is performed to make certain that the output voltage is "high" when the maximum logical "zero" input voltage is applied. Each input is separately biased with the maximum input voltage that will insure "turn-off" of the output transistor. The other inputs are open-circuited or tied to V_{cc}. The output supplies a load which represents the maximum number of logical "one" inputs that the output is expected to load. The logical "one" output voltage, measured from the output pin to ground, is thus a voltage-divider measurement between the "pull-up" resistor and the load resistor. This voltage must be sufficiently high to make sure that the inputs to the next gate (s) are reverse biased.

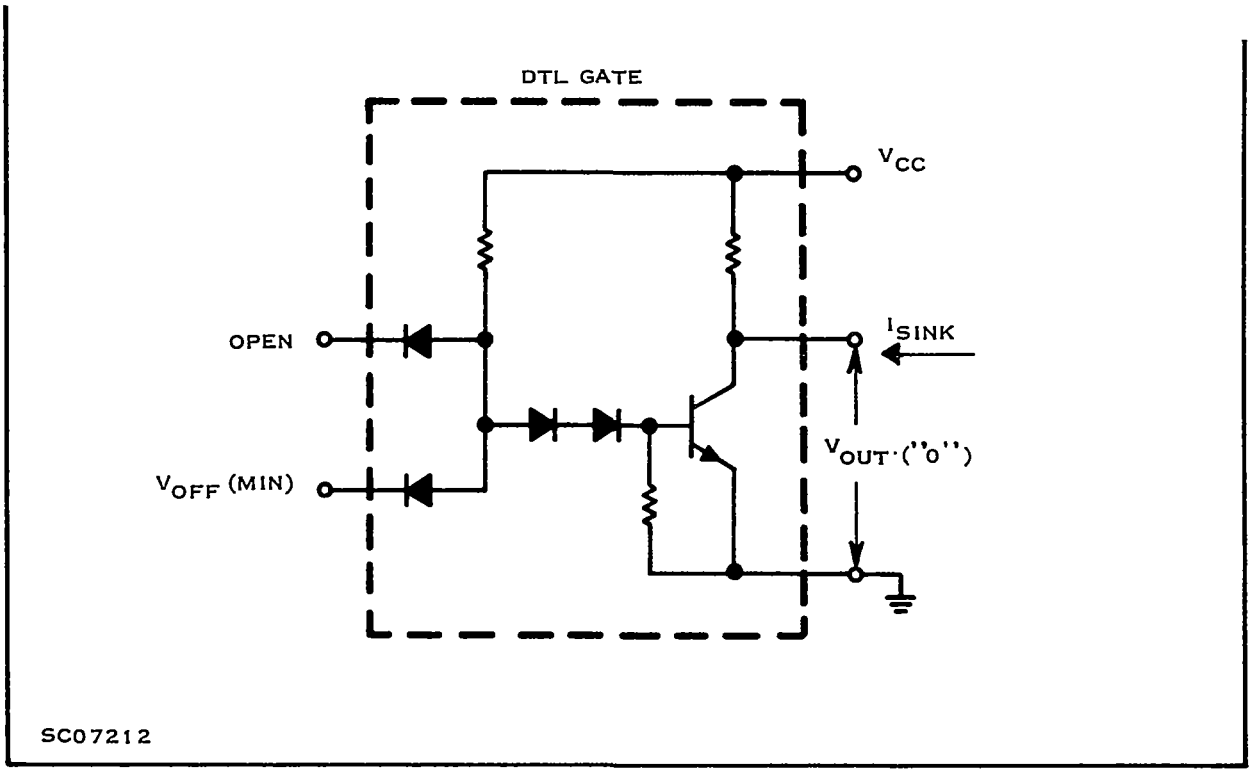

Figure 3-13. "Zero" Output Voltage Measurement Circuit for DTL Device

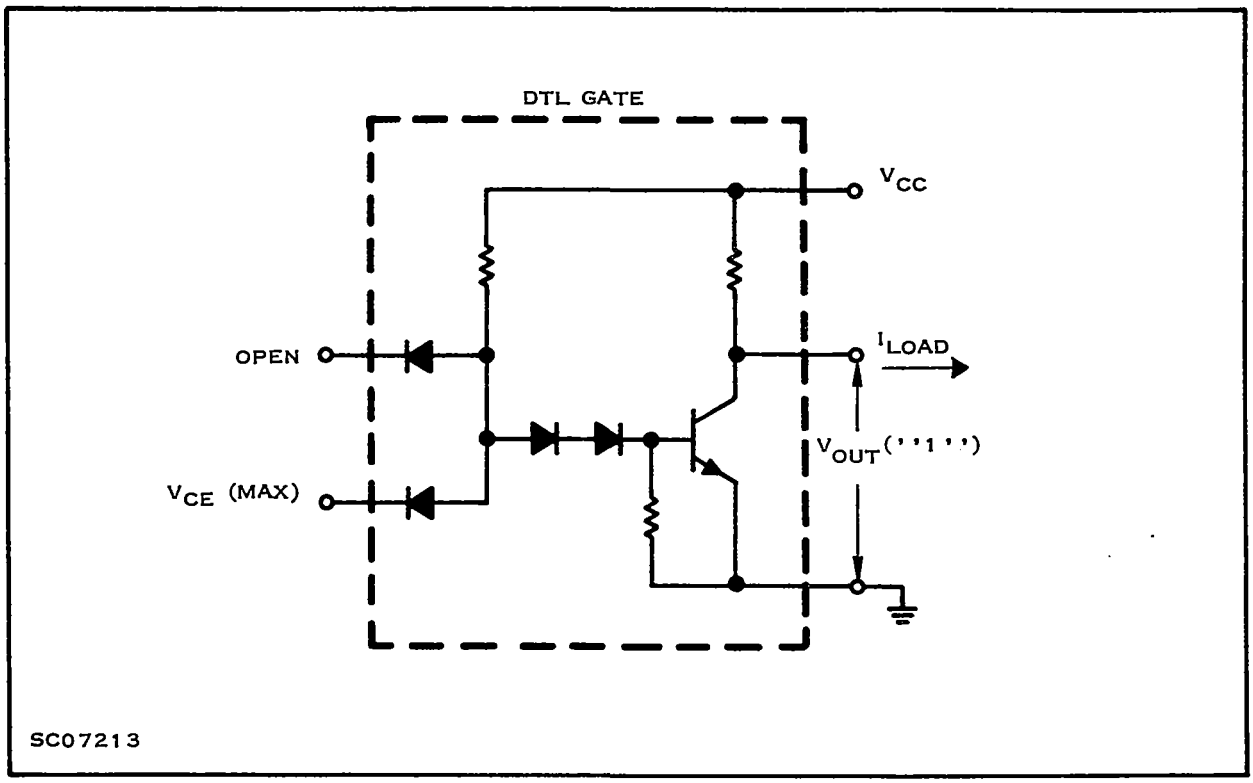

Figure 3-14. "One" Output Voltage Measurement Circuit for DTL Device

The ac or dynamic test, shown in Figure 3-15, merely determines if the device performs the logical "zero" and logical "one" voltage levels at a prescribed repetition rate, and if the logic function changes within a specified length of time.

The equipment required for testing the dc parameters on the DTL logics is:

- One voltmeter with a 0-to-50 V capability and a 10 MΩ or higher input impedance.
- One current meter with a 10 nA-to-30 mA current-range capability.
- Two dc power supplies with variable voltages from 0-to-8 V. Current-limiting characteristics are desirable, but not essential.
- One dc power supply with variable voltage from 0-to-50 V. Current-limiting is desirable but not essential.
- A variable resistor to control sink and load currents.
- A test fixture and sufficient interconnecting cables to connect power supplies and monitoring meters.

In addition to the equipment listed for the dc tests, the following is required for ac parameter measurements:

- One pulse generator with frequency capabilities up to 10 MHz, pulse amplitude of 0-to-8 V, and independent rise and fall time capabilities of 15 ns.
- One syncroscope or dual trace oscilloscope with internal rise time characteristics equal to or less than 15 ns, internal impedance of 1 MΩ or greater, and voltage magnitudes of 0.5 V per cm to 2 V per cm.
- A test fixture.
- Various capacitors, resistors and diodes for loading as prescribed by the individual data sheet or other specification.

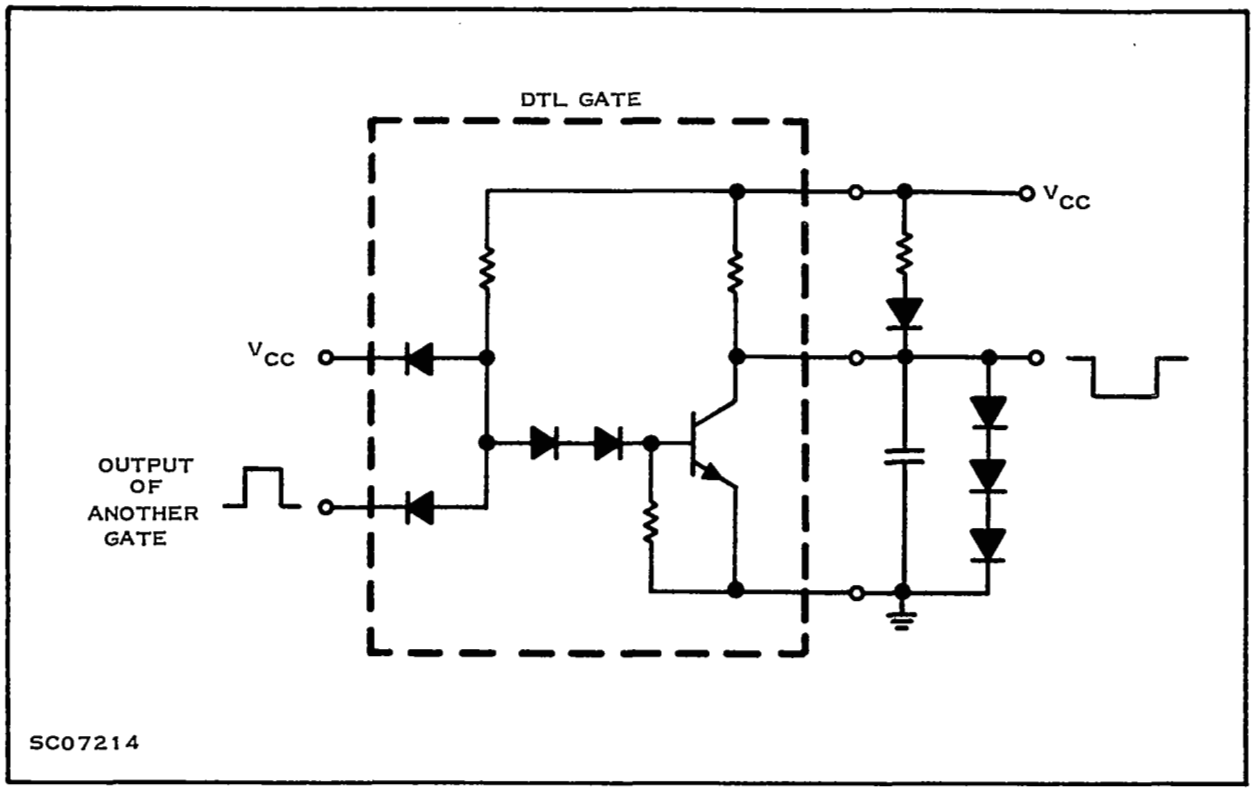

Figure 3-15. Dynamic Test Circuit for DTL Device

(3). Transistor-Transistor Logic. Four basic parameters may be used to determine the operating characteristics of a transistor-transistor logic device. These basic parameters are as follows:

- Input current
- Output voltage
- Output current
- Dynamic test

The normal temperature extremes of operation may be specified from −55°C to +125°C; therefore, the dc parameter tests are usually performed at these extremes to insure proper operation over the entire temperature range.

The input current tests are made with the logic in the logical "zero" condition and in the logical "one" condition. The logical "zero" input current is that current which is required in order to insure that there will be a logical "zero" condition at the output. The test is shown in Figure 3-16; it is performed under worst-case condition, i.e., each input is placed at the maximum "off" voltage level that may be applied by a preceding logic. The remaining inputs are grounded. The input under test is reverse biased; however, the multiple emitters exhibit parasitic transistor

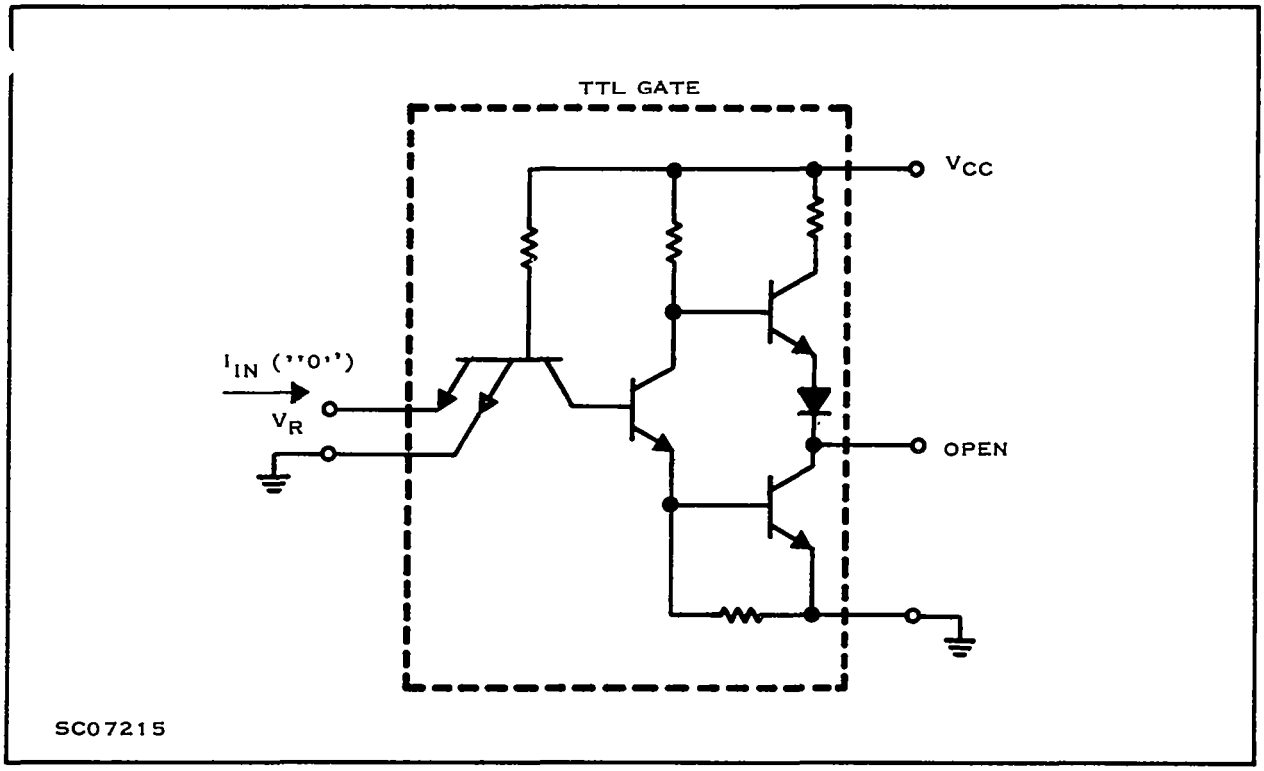

Figure 3-16. "Zero" Input Current Measurement Circuit for TTL Device

characteristics which allow a leakage current to exist which is higher than reverse leakage. The parasitic current is the base-emitter injected current multiplied by the gain of the parasitic transistor. The gain of the parasitic transistor is quite low (below 0.05) but a 1 mA base-emitter current is sufficient to allow 50 μA of logical "zero" input current to be measured. Typical logical "zero" currents are 5 μA to 15 μA per unit. The logical "one" input current is that current required by an input to insure a logical "one" condition at the output. The test (Figure 3-17) is performed at the worst-case condition, i.e., the applied input voltage is assumed to be a maximum V_{CE} of a preceding logic. All other inputs are tied to V_{CC}. Specified limits are determined from worst-case design tolerances.

The output voltage tests are also made with the logic in the logical "zero" and in the logical "one" conditions. The logical "zero" output voltage (Figure 3-18) must be "low" enough to insure the "turn-off" of any other TTL gate that it controls. It must be able to sink current from 10 other logical "one" inputs. This output voltage is the V_{CE} of the "low" side transistor. The logical "one" output voltage (Figure 3-19) must be "high" enough, when applied to the input of another TTL, to insure "turn-on" of the TTL it controls. The output "off" voltage must be capable of loading 10 other gates. The resistance of the output load is selected to insure the loading of 10 logical "zero" input currents. The output voltage is read with each input at logical "zero," while the other inputs are taken to V_{cc} (worst case).

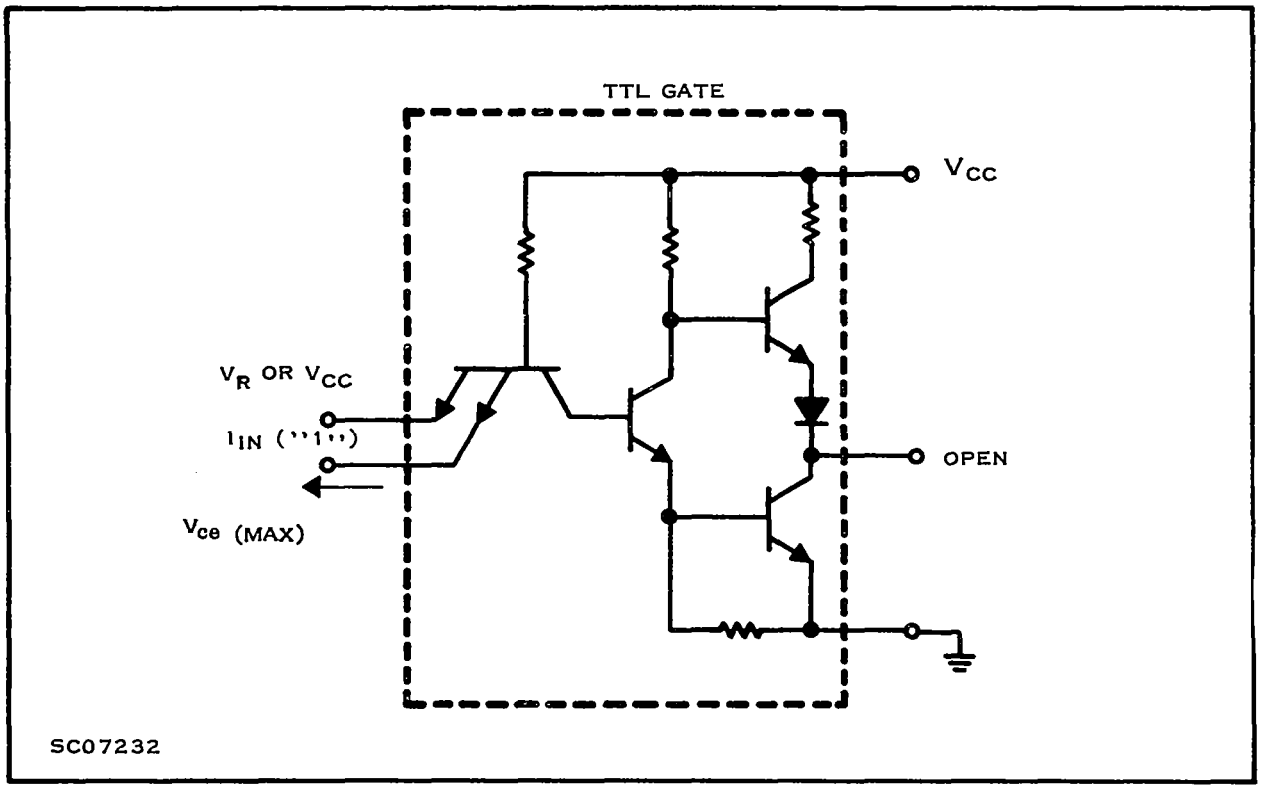

Figure 3-17. "One" Input Current Measurement Circuit for TTL Device

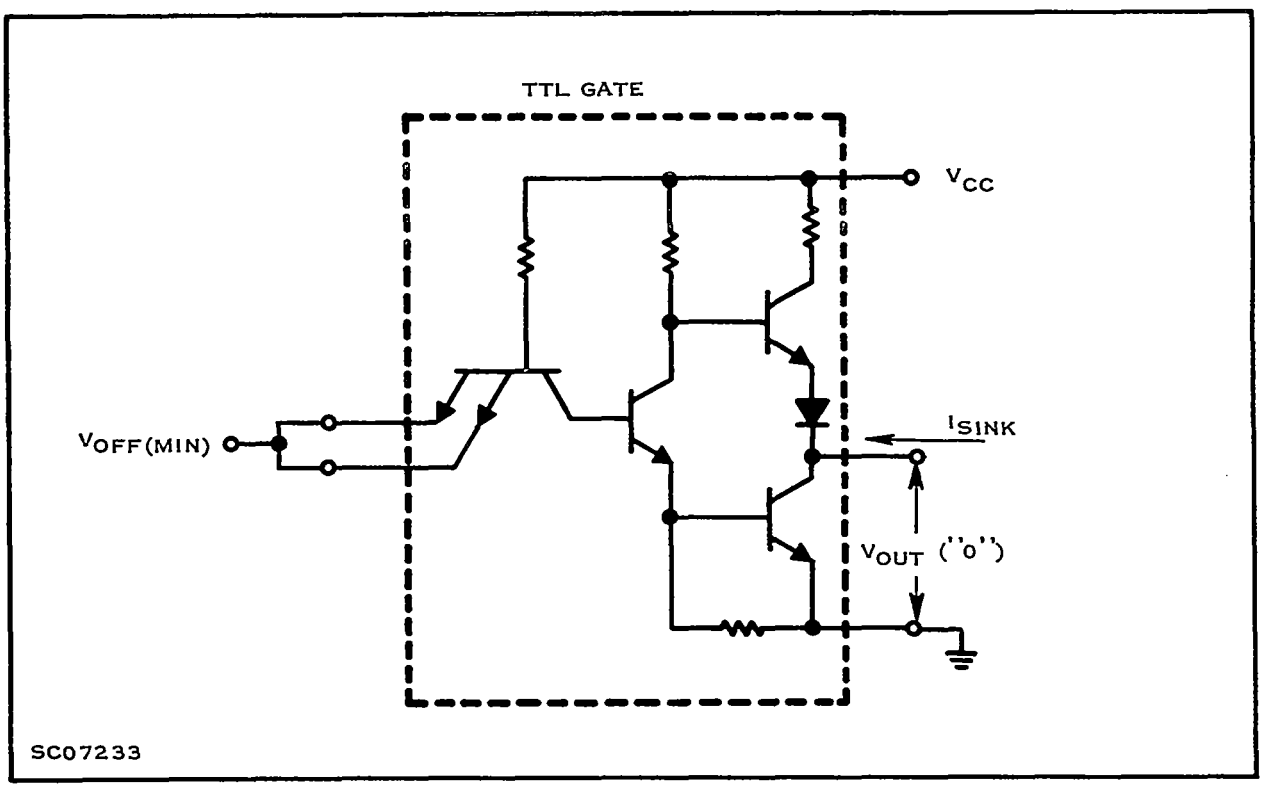

Figure 3-18. "Zero" Output Voltage Measurement Circuit for TTL Device

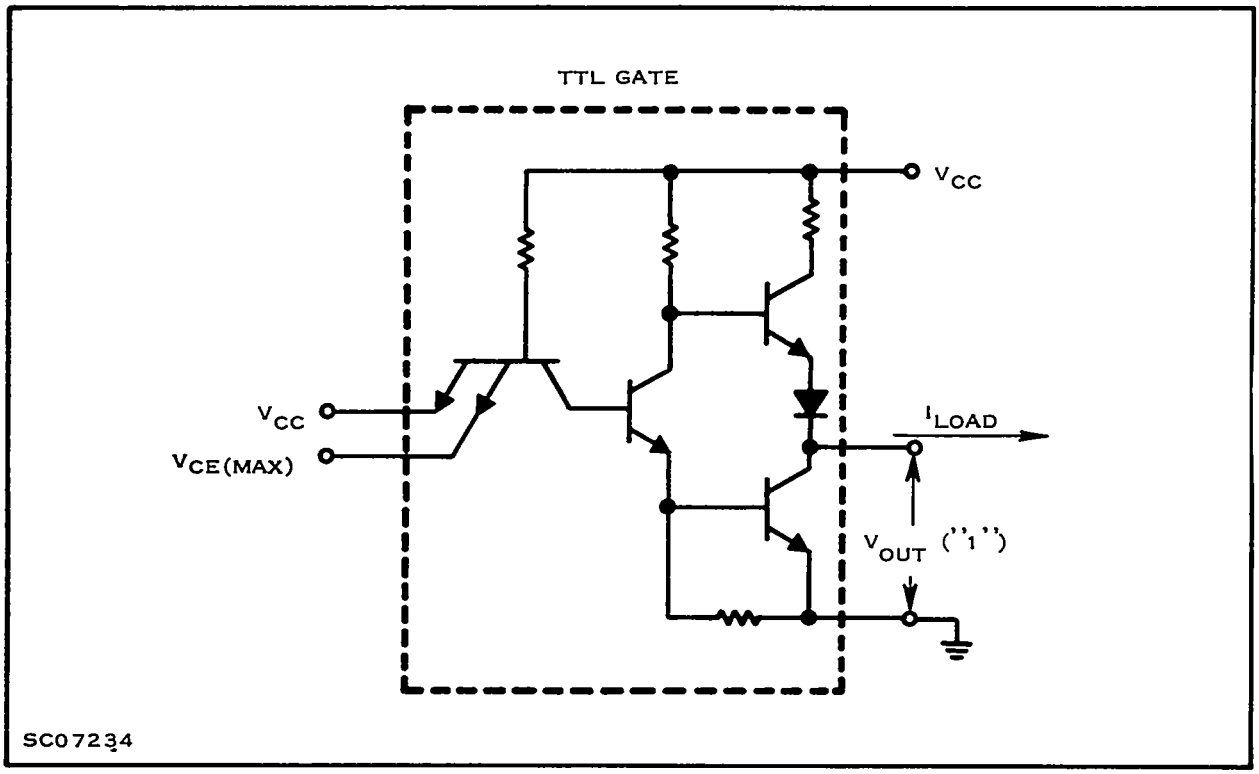

Figure 3-19. "One" Output Voltage Measurement Circuit for TTL Device

The short-circuit output current is measured by means of the test circuit shown in Figure 3-20, to determine the impedance of the output in the logical "one" condition. The current measurement is made at the output, with the output grounded through a current meter. The inputs are taken to logical "zero" to insure that the V_{off} transistor is conducting.

The circuit for the dynamic test is shown in Figure 3-21. This test determines if the device performs the logical "zero" and logical "one" functions at a prescribed repetition rate. The dynamic test also determines if the logic function changes within a specified length of time. The TTL performs high-speed switch functions with propagation delay time in the range of 10 ns, and frequency capabilities in the range of 25 MHz.

Equipment for testing the dc parameters of the TTL device is as follows:

- One voltmeter with a 0-to-10 V capability and a 10-MΩ or higher input impedance.
- One current meter with a 1 μA-to-100 mA current range capability.

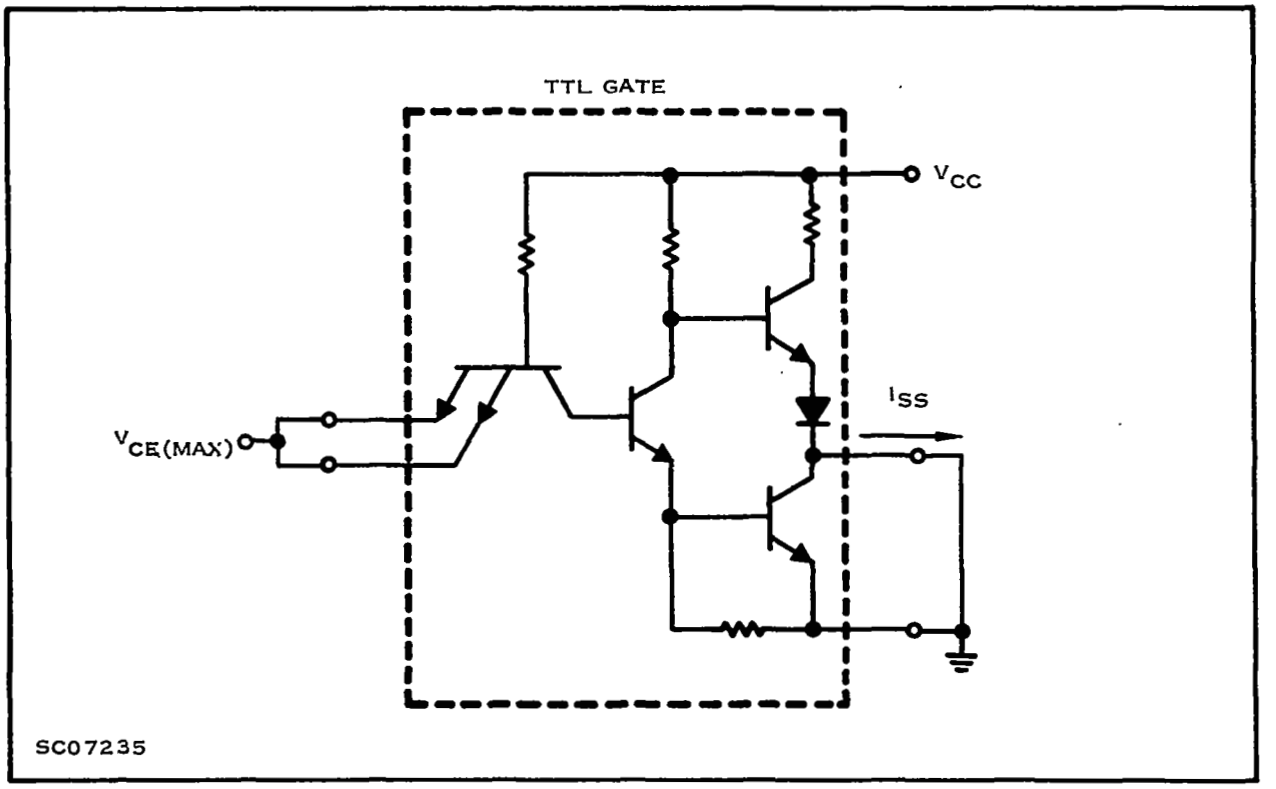

Figure 3-20. Short-Circuit Output Current Measurement Circuit for TTL Device

- Three dc power supplies with variable voltages from 0-to-8 V. Current-limiting capabilities are desirable, but not a necessity.
- A test fixture and sufficient interconnecting cables to connect power supplies and monitoring meters.
- Variable resistors for loading.

In addition to the equipment listed for the dc tests, the following is required for ac parameter measurements:

- One pulse generator with frequency capabilities up to 25 MHz, pulse amplitude of 0-to-8 V, and independent rise and fall time capabilities of 15 ns.
- One syncroscope or dual trace oscilloscope with internal rise time characteristics equal to or less than 15 ns, internal impedance of 1 MΩ or greater and voltage magnitudes of 0.5 V per cm to 2 V per cm.
- A test fixture.
- Various capacitors, diodes, resistors and transistors to furnish an ac load to the outputs. (Alternating-current loading is shown on individual data sheets.)

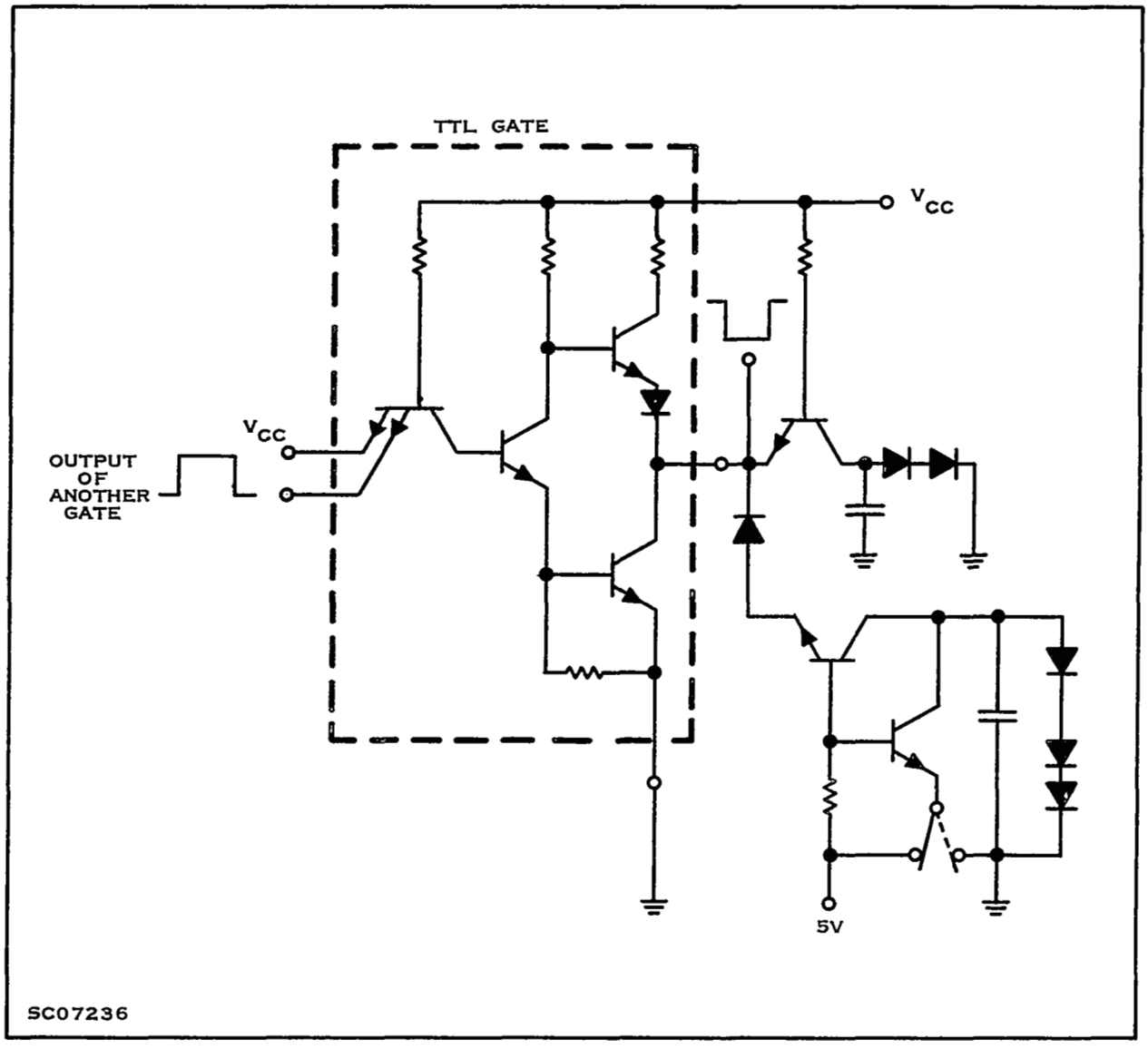

Figure 3-21. Dynamic Test Circuit for TTL Device

b. Linear Devices

(1). General. The more common parameters which determine the operating condition of linear microcircuits are discussed here.

(2). Direct-Current Parameters. Three dc parameters will be briefly described here. The test circuit for the first two parameters is shown in Figure 3-22. Before a parameter test is performed, the device is first balanced by adjusting R_9 to obtain a voltage difference of 10 mV or less between output pins 8 and 13.

"Differential input voltage offset" (DIVO), is measured at pin 7 (Figure 3-22). This parameter indicates the voltage required to balance the device. Its nominal values are in the range ±0.5 mV.

The parameter, "common mode output voltage offset" (CMOVO), indicates the voltage of the balance point above or below ground. This parameter is measured at pin 8 (Figure 3-22); its nominal values are in the range ±0.5 mV.

The test circuit shown in Figure 3-23 is used to measure "differential input current offset" (DICO). This circuit is balanced in the same manner as the previously described circuit. Parameter DICO is a measure of the input current at pin 7 required to balance (by adjusting R_9) the test circuit. It is calculated by the formula:

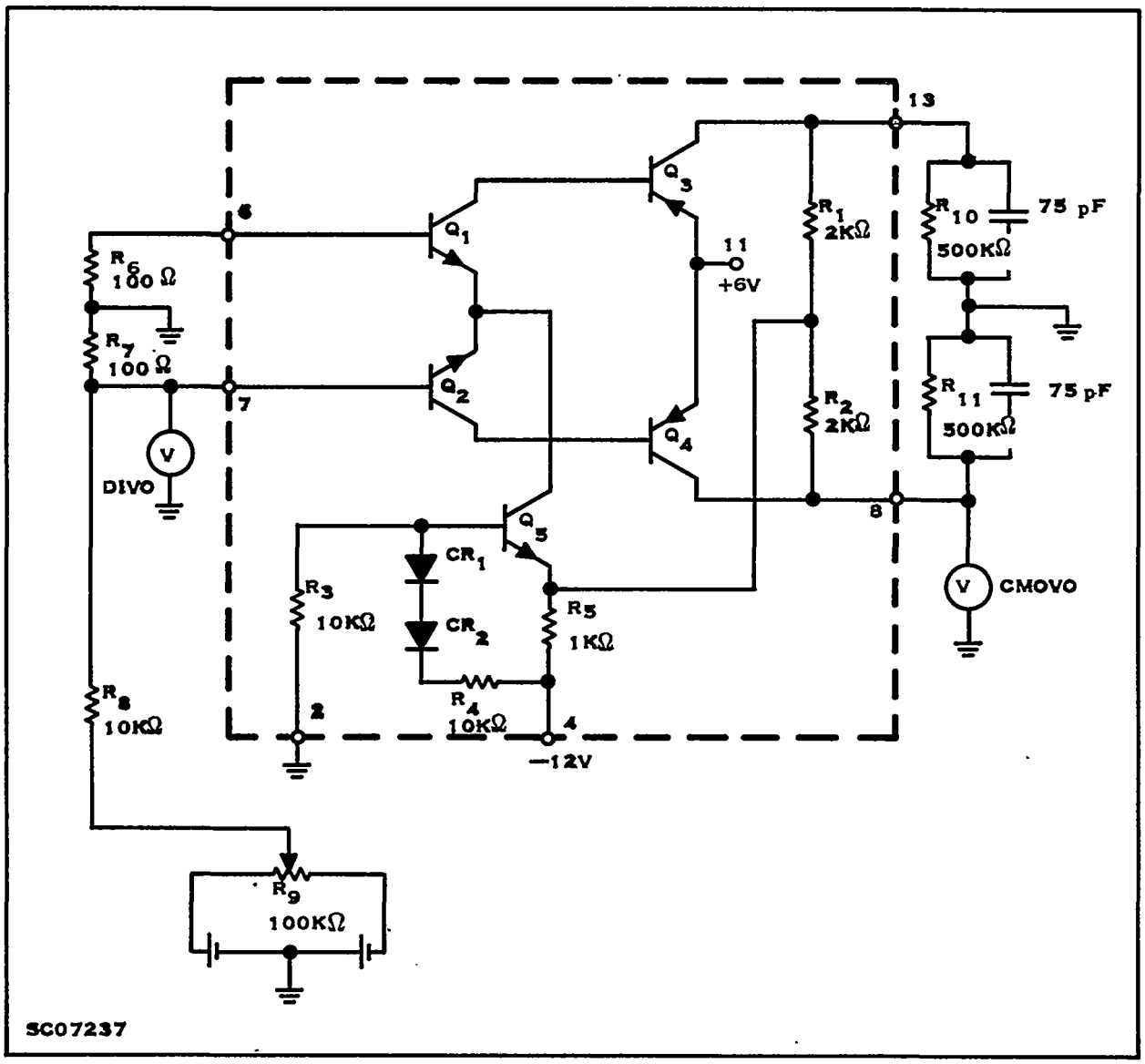

Figure 3-22. Differential-Amplifier DIVO and CMOVO Measurement Circuit

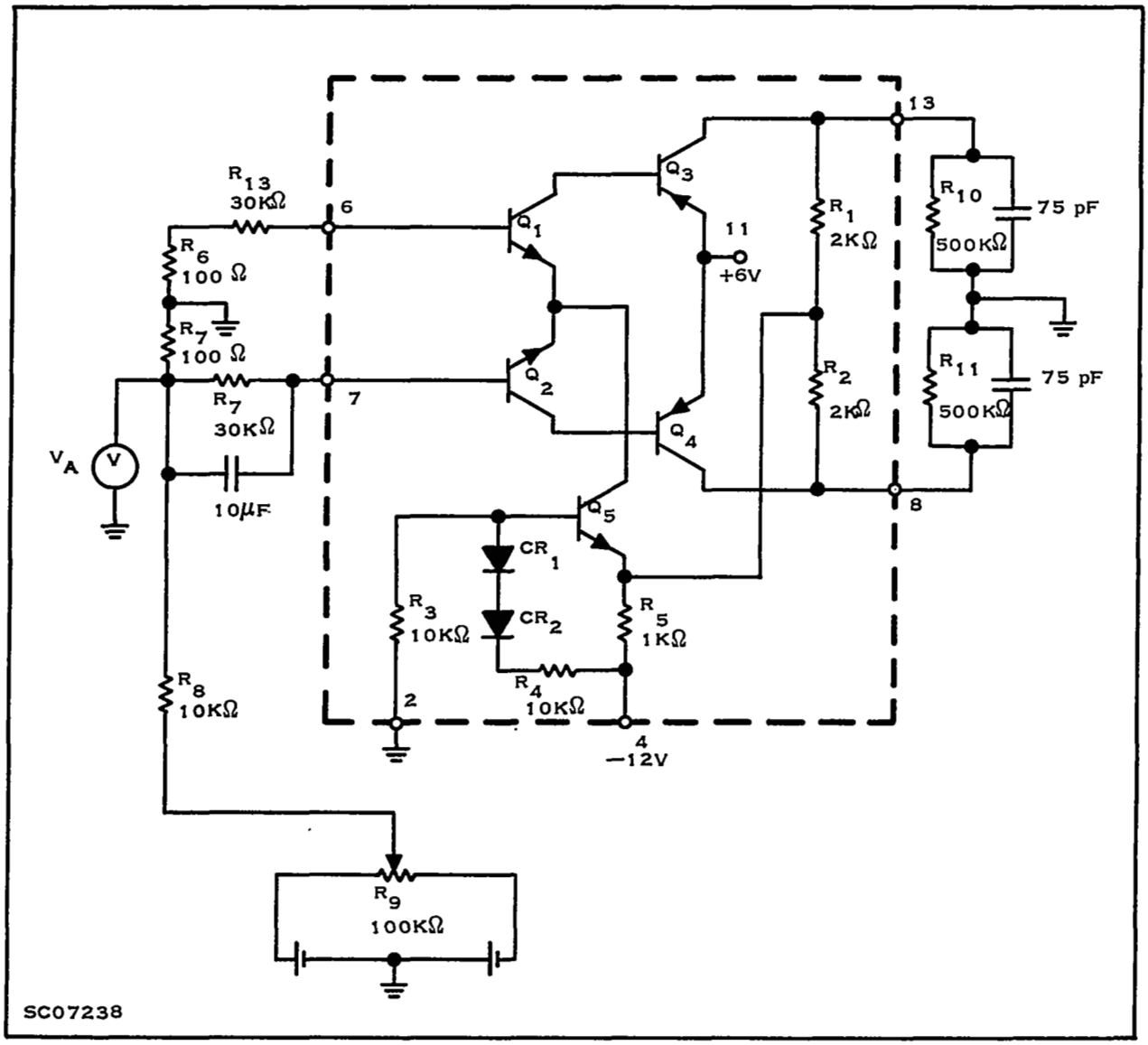

Figure 3-23. Differential-Amplifier VA Measurement Circuit for DICO Calculation

$$DICO = \frac{V_A - DIVO}{R_{in}}$$

where

V_A = voltage at point "A" when balanced

$R_{in} = R_{12}$, 30 k Ω

(3). Alternating-Current Parameters. The three ac parameters to be presented here are measured after the device has been balanced in the manner described for measuring dc parameters. The test circuit is shown in Figure 3-24.

The parameter, "voltage gain" (GV), is the ratio e_{out}/e_{in}. A 1000-Hz, 1-mV rms sine wave is required for e_{in}. Nominal gain is 200.

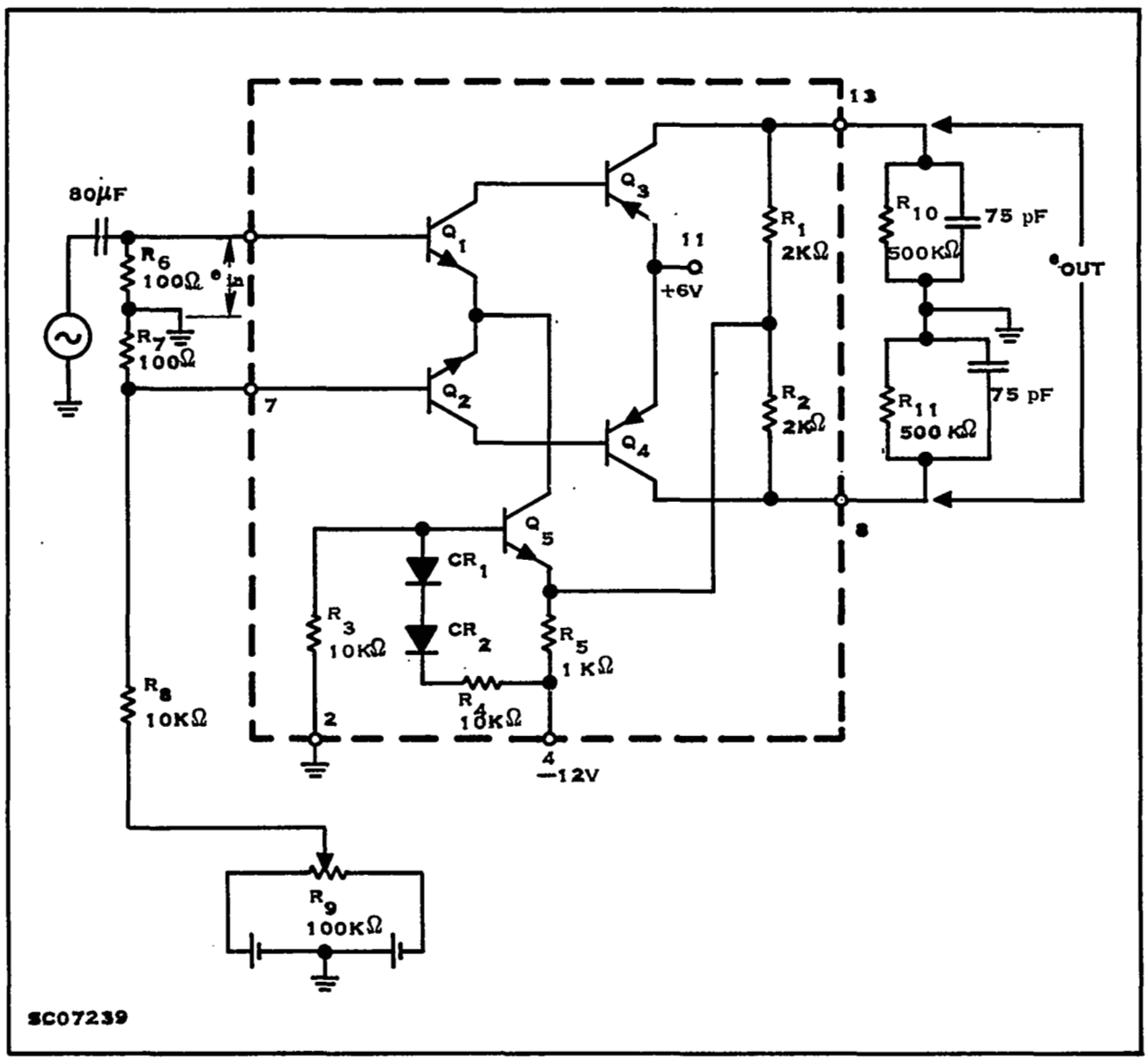

Figure 3-24. Differential-Amplifier Voltage Gain (GV), AC Signal Swing (ACSS), and Upper Frequency Cutoff (fh) Measurement Circuit

To measure ac signal swing (ACSS), increase e_{in} until the e_{out} sine wave starts to clip at the positive or negative peaks. Nominal ACSS is 20 V peak-to-peak.

"Upper frequency cutoff" (fh), is measured by increasing the frequency of e_{in} until e_{out} is down 3 dB from the 1000 Hz level. The nominal fh frequency is 200 kHz.

The equipment necessary to conduct these parameter measurements is:

- Current-limited, ac power supplies with voltage variable from 0-to-12 V.
- VTVM type meter capable of current measurements.
- An oscilloscope with dual traces and capabilities of 1 mV/cm vertical sensitivity, 1 MΩ input impedance.
- Signal generator with frequency range of 1-to-200 kHz sine wave output.

(4). Conclusions. Test boxes may be constructed to coordinate all the equipment with the unit under test. "Bread boarding" may be used to make the connections although this is not advisable with linear circuits, since parasitic oscillations may occur, particularly with high-gain, wide-band amplifiers. Certain ground rules will help in decreasing the chances of these oscillations. Where power supplies are connected, use a filter composed of a series choke followed by a ceramic type capacitor to ground. This will decrease any feedback through power supplies. Keep signal-carrying lead wires short and avoid paralleling of leads, in order to prevent "cross talk." Shielded cable is useful as long as the terminating impedance is low; otherwise, cables must be frequency-compensated. Complex switching will allow a large number of parameters to be measured and may even allow a variety of similar linear circuits to be measured with the same test box, but care must be taken, since the complexity of the circuit may give untold problems with oscillation and "cross talk."

3. Data Correlation

After the previously described parameter tests have been performed, the resulting test data must be compared with the failure information received with the device. If correlation exists, it may be assumed that the failure information is correct, and further tests to isolate the problem may be made. Exact correlation on parameter values may not be expected, but the test results usually should fall within the normal range of parameter drift and the accuracy tolerance of the test equipment.

If correlation does not exist, careful retesting and observation of parameter behavior is necessary. If correlation still does not exist, a careful analysis of the results obtained is required.

Agreement of test data and failure information in major areas that would cause device failure, but disagreement in other areas, would warn the analyst that the device characteristics may have changed through testing, continued use in a system, or improper handling following initial failure. The primary failure mode may thus be masked by new indicators generated by the primary failure mode.

If complete lack of data correlation exists (this would indicate the microcircuit failed in a manner other than that reported in the preliminary information), further tests must be made to determine if the device's characteristics have changed as previously discussed or if the failure information may have been erroneous.

If lack of correlation indicates the device is not a failure, further tests must be made to determine if initial information was erroneous or if an intermittent problem exists.

4. Handling of Nonverified Failures

Devices which have been removed from test or circuit application as defective and which subsequently test good are classified as nonverified failures. These devices may have failed due to intermittent conditions existing within the devices or they may have been mistakenly identified as failures.

The analysis of nonverified failures often leads to inconclusive results. The success of an analysis of nonverified failures depends on 1) the quantity and accuracy of electrical symptoms obtained during circuit application or test, and 2) a proper evaluation of information obtained from tests performed by the analyst.

The analyst is limited only by the fact that the failure symptoms no longer exist. The laboratory tests described hereafter are essential to definitive analysis of nonverified failures.

a. Application Evaluation

The device in question should, whenever possible, be operated by the analyst in a test circuit or application which simulates the failure conditions. A simulated test condition provides the analyst with a concise knowledge of the device in its application and enables him to determine that the device in its present condition does or does not perform satisfactorily. He should also evaluate the device for marginal worst-case design conditions such as the device's sensitivity to power supply voltages, input signals, frequencies, clock responses, loading, etc.

b. Temperature Cycle

Failure symptoms can sometimes be reproduced by varying the ambient temperature of the device while monitoring the functional characteristics. Temperature cycling should not exceed the specified temperature range.

c. Vibration

Intermittent conditions can also be reproduced by monitored vibration testing. A 60-cycle vibration in the range of 30-to-50 gravity units is recommended. Care should be taken to see that the contacts between the device under test and the test fixture do not introduce spurious results.

d. Visual Examination

Visual examination of the internal portion of the device should be performed only after all electrical information has been obtained. Internal electrical probing may be desirable if the original failure symptoms were reproduced. In any case, the device should be examined visually for defects which would have caused the failure symptoms originally observed.

e. Conclusions

Conclusions drawn by the analyst of nonverified failures may be misleading unless they are properly interpreted. These conclusions should, therefore, be weighted by the degree of confidence produced by failure symptoms and laboratory test results.

C. PRELIMINARY ELECTRICAL TESTS

1. Isolation and Threshold Tests, Equipment Required

In addition to the parameter tests, a case-isolation test is frequently performed to provide more information concerning the present condition of the device. This test determines if the case is electrically isolated from all the external pins and the silicon bar. Case isolation is checked by placing a voltage (15 V is frequently used) between the case of the device and its external terminals. The resulting characteristic is viewed on a curve tracer. A horizontal trace indicates no shorting to the case, while a vertical line indicates that one or more leads or the bar are shorted or leaky to the package. If the latter occurs, each terminal is checked individually to locate the defect. When the bar is shorted to the case, one polarity of voltage may cause leakage while the opposite will not. Thorough testing utilizes both polarities. Some bars and external leads are purposely connected to the case. Knowledge of device construction prevents confusion in this instance.

Another test which is very helpful in determining device condition is a threshold test. This is merely performing a continuity test at each external terminal to ascertain if electrical connection to the silicon bar does exist. The technique consists of forward-biasing the substrate of the silicon bar with respect to the other elements, and using a curve tracer. The resultant forward-diode characteristic is the clue to an open bond. If a bond to the substrate or other element involved is open, the trace is a horizontal line. If the trace is that of a normal forward-diode (or diodes), the bonds involved are intact. Some external pins are connected to the substrate purposely by resistors or other than by single diodes. This circuitry should be considered when performing threshold tests. Low potentials should be utilized to avoid "snapping-in" open bonds. Voltages higher than 1 V have been observed to cause open bonds and other open circuits to become good.

Isolation and threshold tests are most conveniently performed by use of a curve tracer. These may be purchased ready made or a useable substitute may be constructed for use with an oscilloscope which has an external horizontal deflection input. A schematic of such a substitute is shown in Figure 3-25.

2. Pin-to-Pin Measurements and Parasitic Effects

a. Digital Devices

The information to be gained from pin-to-pin measurements (curve tracer analysis) can be invaluable for evaluation of defective devices. Curve tracer analysis utilizes trace characteristics to evaluate component paths between two pins. The equipment required consists of the following:

- A curve tracer (Tektronix 575 or equivalent).
- A unit fixture or fingerboard.
- A test box with which to connect any pin combination of the device to the curve tracer.
- Three test leads of suitable length.

The technique of curve-tracer analysis will be illustrated with the aid of Figure 3-26, which shows a diode and a resistor connected in parallel between pins 1 and 2. The voltage-to-current relationship existing between these pins may be obtained by applying a voltage-current curve tracer to the two pins. The trace obtained would depend on the polarity used when applying the voltage. The trace expected to be obtained would be as shown in Figure 3-27, if a positive (+) voltage were applied at pin 1 with respect to pin 2. A straight line, indicating a resistance with the value of V/I, is obtained until the forward-diode threshold is reached. The curve or trace then changes to become the forward-diode resistance (very low) in parallel with

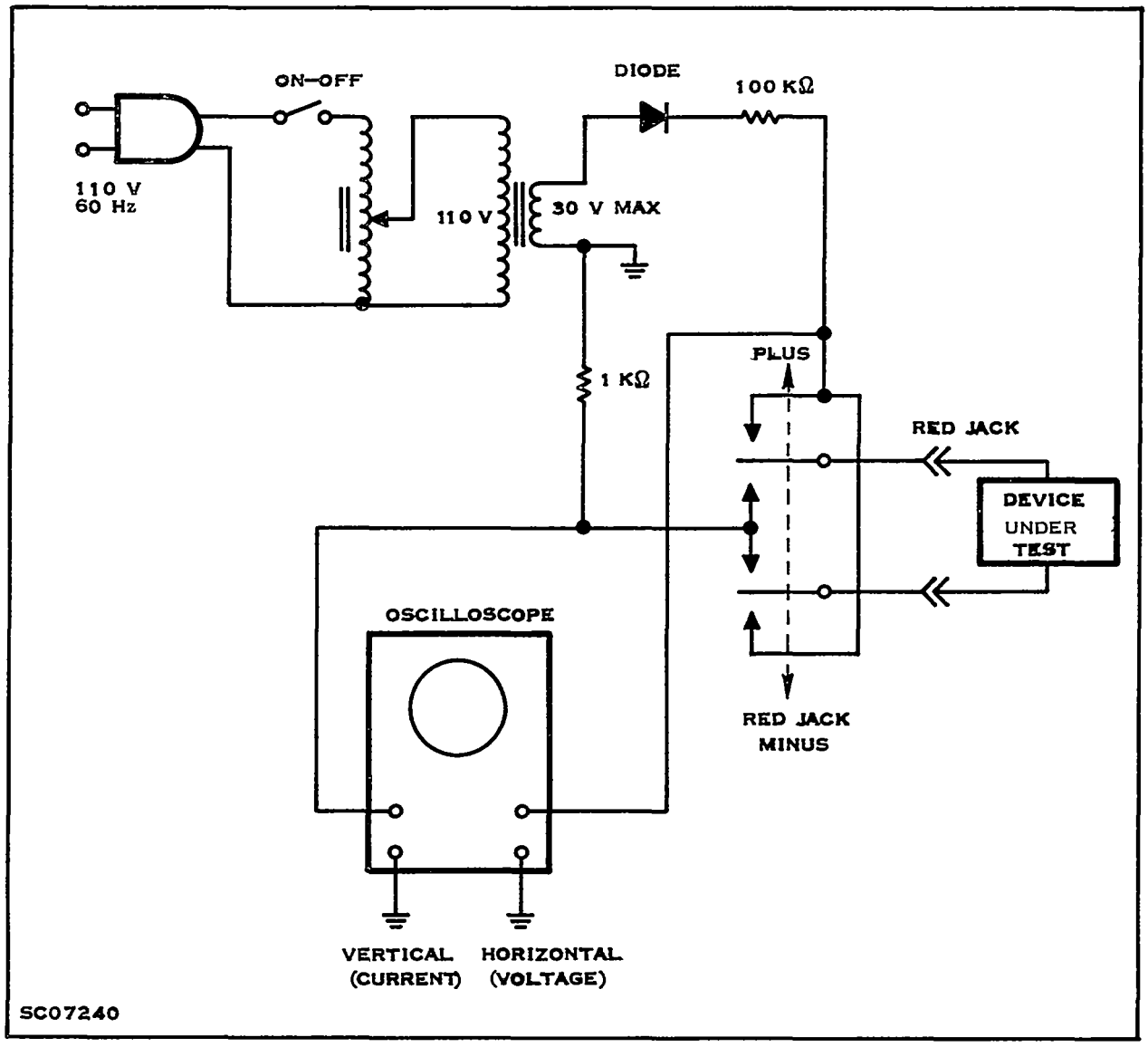

Figure 3-25. Curve Tracer Circuit

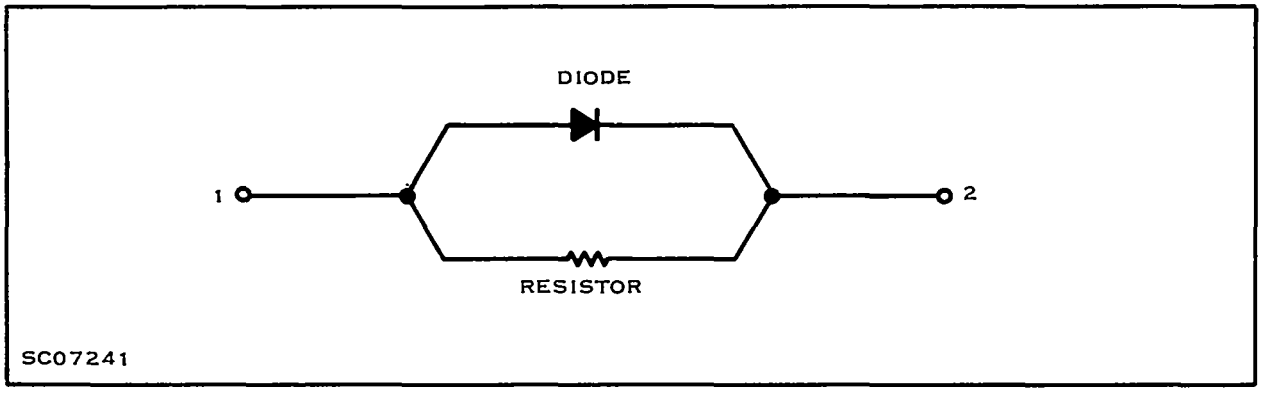

Figure 3-26. Circuit Example for Curve Tracer Test

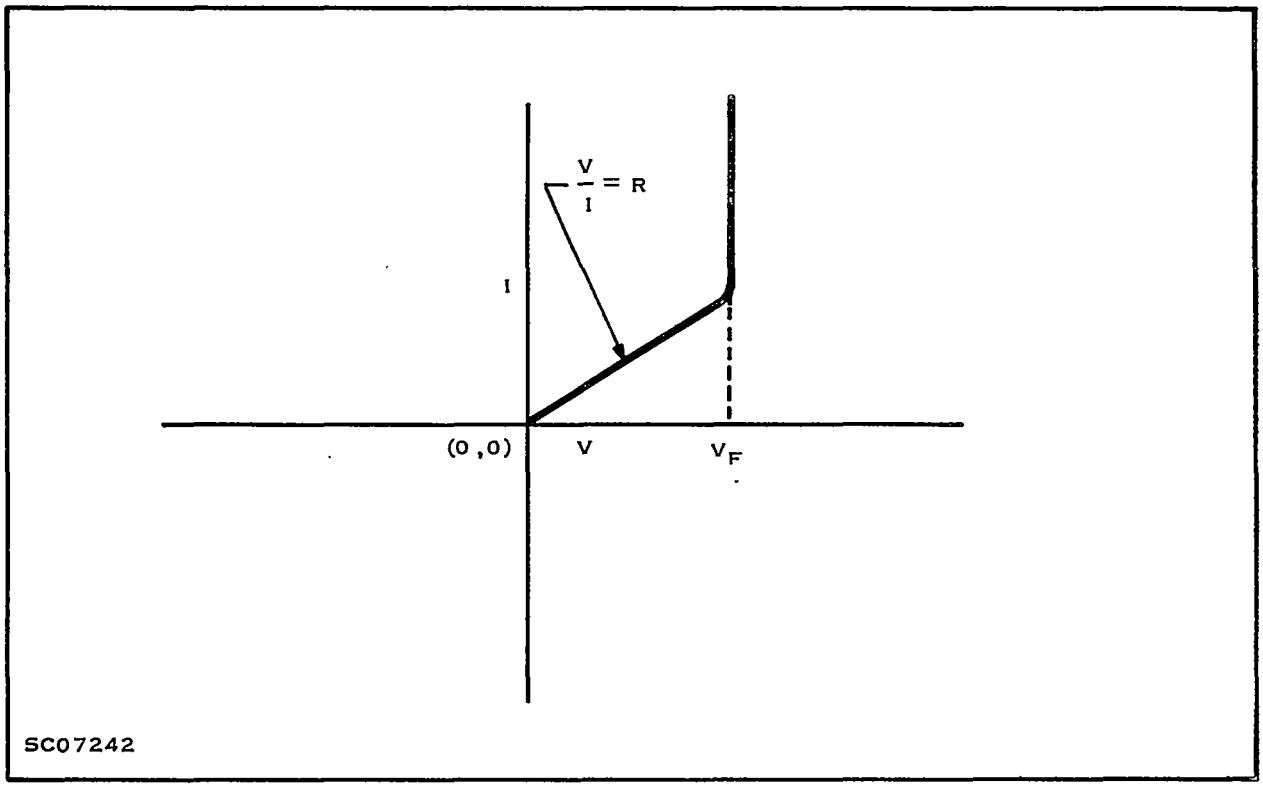

Figure 3-27. Curve Tracer Display with "Plus" Polarity on Pin No. 1 of Circuit Shown in Figure 3-26

the resistance value. If a positive (+) voltage were applied at pin 2 with respect to pin 1, the trace expected to be obtained would be as shown in Figure 3-28. A straight line (indicating a resistance with the value of V/I) is obtained until the reverse breakdown voltage of the diode is reached. The curve or trace then changes to become the diode avalanche resistance in parallel with the resistor. Thus, the following information could be obtained by evaluation of the two traces:

- The V_F value of the diode.
- The V_R value of the diode.
- The resistance value of the resistor.

The actual mechanics of curve-tracer analysis is quite simple and requires little technical skill; however, the interpretation of the information derived requires knowledge of monolithic microcircuit design. This can be illustrated by an example. The circuit schematic of an RCTL gate is shown in Figure 3-29. The input to the gate is a simple R-C network which feeds the base of the output transistor. The resistor is used to limit the base drive, and the capacitor serves to speed up the logic function. The transistor output is "high" or "low," depending on the input voltage

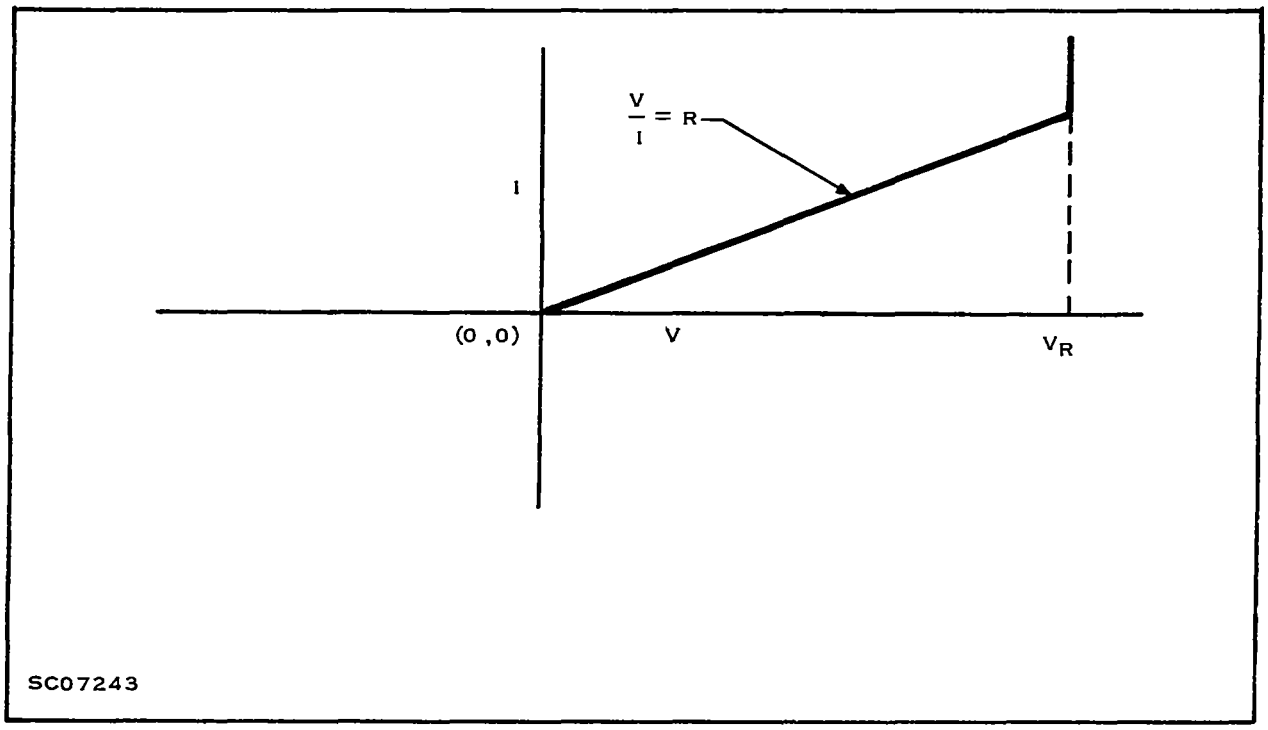

Figure 3-28. Curve Tracer Display with "Plus" Polarity on Pin No. 2 of Circuit Shown in Figure 3-26

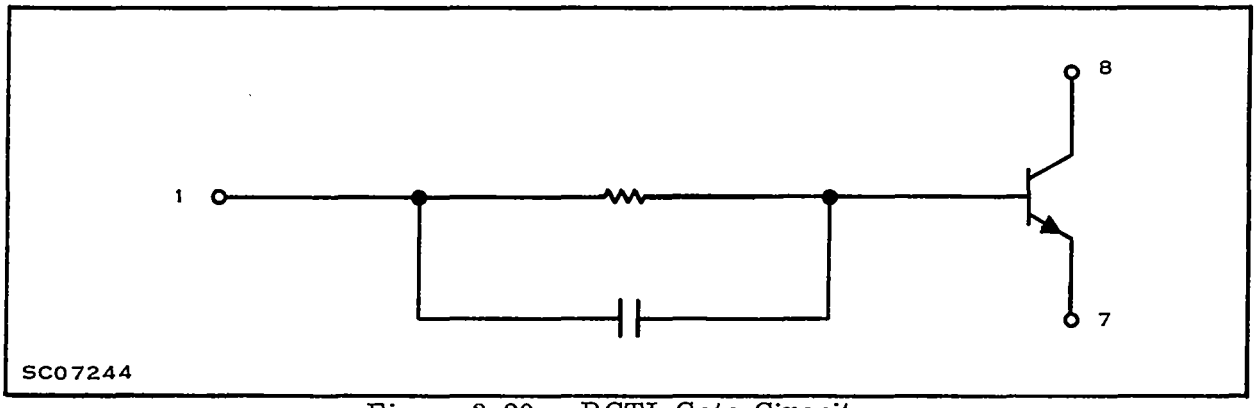

Figure 3-29. RCTL Gate Circuit

applied at pin 1 with respect to pin 7. With pin 1 positive with respect to pin 7, the expected trace characteristic on the curve tracer would be as shown in Figure 3-30. No current would be expected to show on the trace until the forward threshold voltage (V_F) is reached. The trace would then be expected to change to a V/I relationship representing the value of the resistor. The capacitor would not be expected to affect the trace, but this expectation would not be correct. The trace that would actually be obtained would be as shown in Figure 3-31. The difference between the expected trace of Figure 30 and the actual trace obtained in Figure 3-31 is the breakdown of the capacitor, which occurs at a relatively low voltage ($\approx$ 10 V). The RCTL monolithic microcircuit capacitor is a transistor diffusion in a basic substrate material: the collector

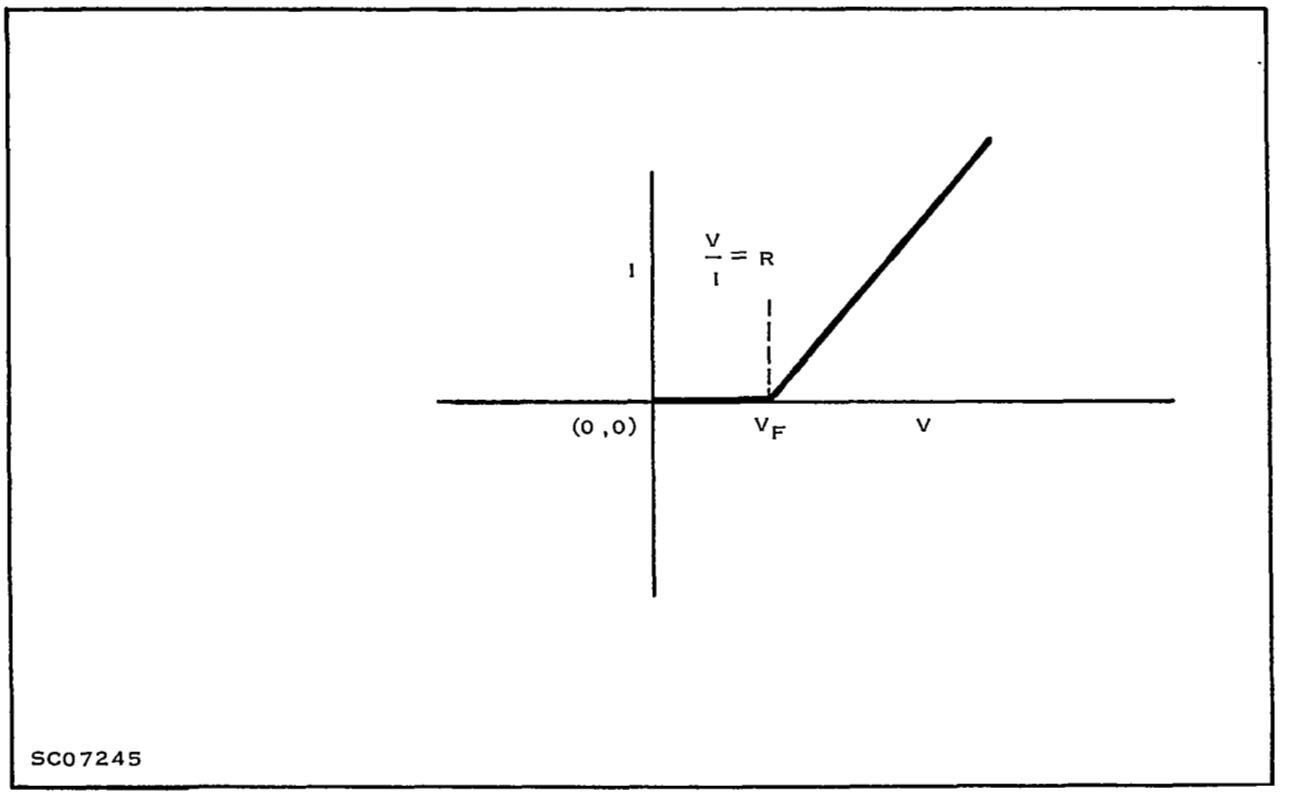

Figure 3-30. Expected Curve Tracer Display with "Plus" Polarity on Pin No. 1 of RCTL Gate

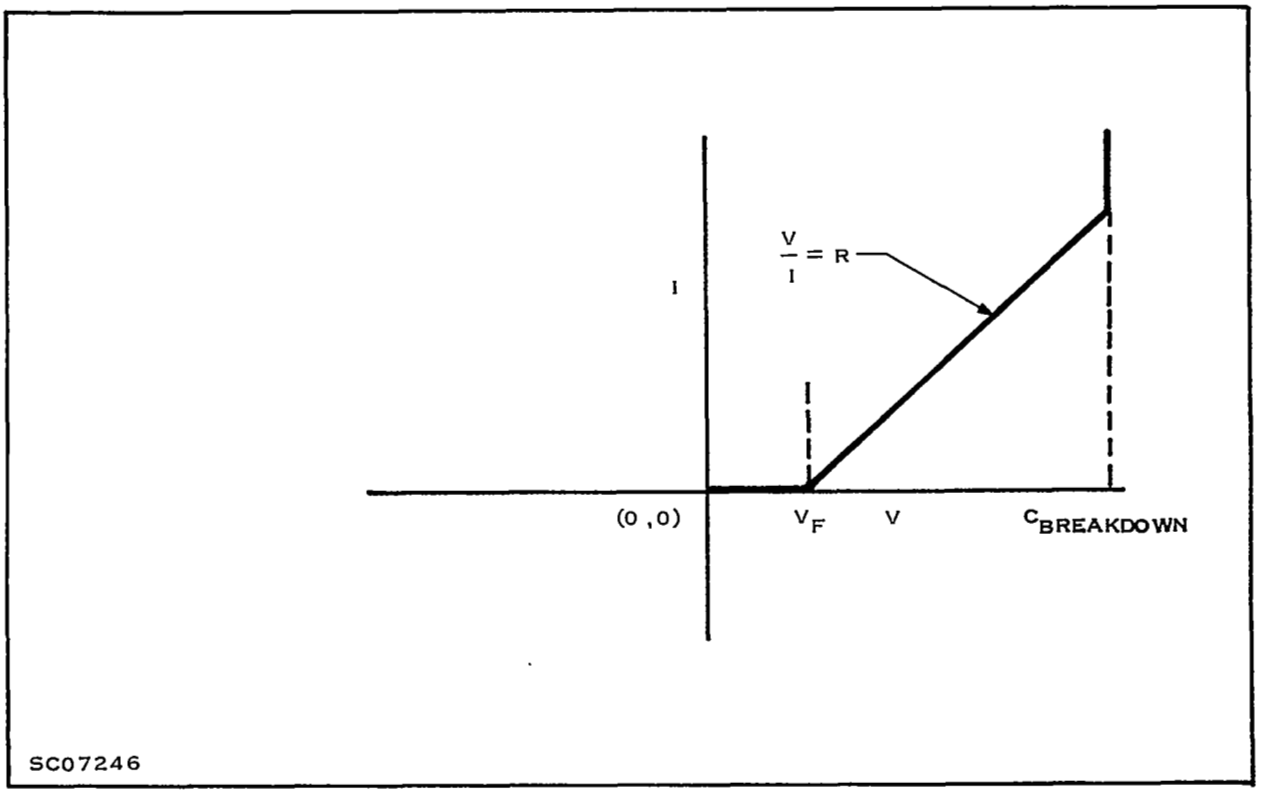

Figure 3-31. Actual Curve Tracer Display with "Plus" Polarity on Pin No. 1 of RCTL Gate

and emitter are tied together by evaporated leads to serve as one plate of the capacitor, while the base serves as the other plate. The capacitance is the sum of the collector-base capacitance and the emitter-base capacitance. The value of capacitance is proportional to the junction areas. The RCTL input circuit with the "revised" capacitor is shown in Figure 3-32. The "C" breakdown of Figure 3-31 occurs at the reverse emitter-base breakdown voltage of the transistor which serves as a capacitor.

Reversing the polarity of the voltage so that a positive voltage is applied to pin 7 with respect to pin 1, and using the circuit of Figure 3-29 for interpretation, the expected trace characteristic would be that of Figure 3-33. This represents the reverse breakdown voltage of the emitter-base diode of the transistor, which becomes a resistance line V/I representing the resistance of the input resistor. Knowledge of the capacitor construction would cause these expected results to be revised, and the circuit of Figure 3-32 rather than Figure 3-29 would be used. The current would then be expected to by-pass the resistor through the forward-biased base-collector and base-emitter diodes of the capacitor. The revised evaluation with pin 7 positive (+) with respect to pin 1 would cause one to expect the trace characteristic shown in Figure 3-34. This would also be incorrect. Pin 7 of the RCTL monolithic microcircuit is tied to substrate material (device ground). The resistor is an "N" diffusion into the basic "P" substrate material. Current would, therefore, flow from

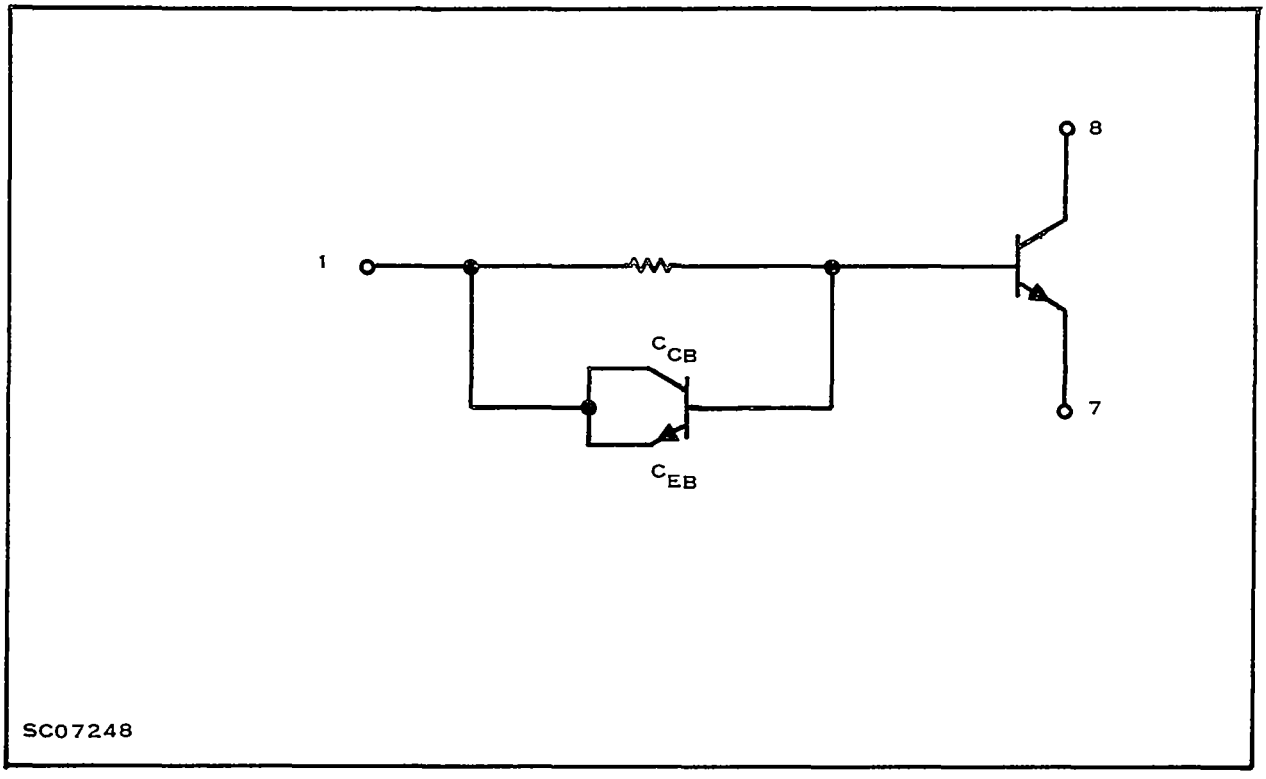

Figure 3-32. RCTL Gate with Capacitor Drawn as Constructed

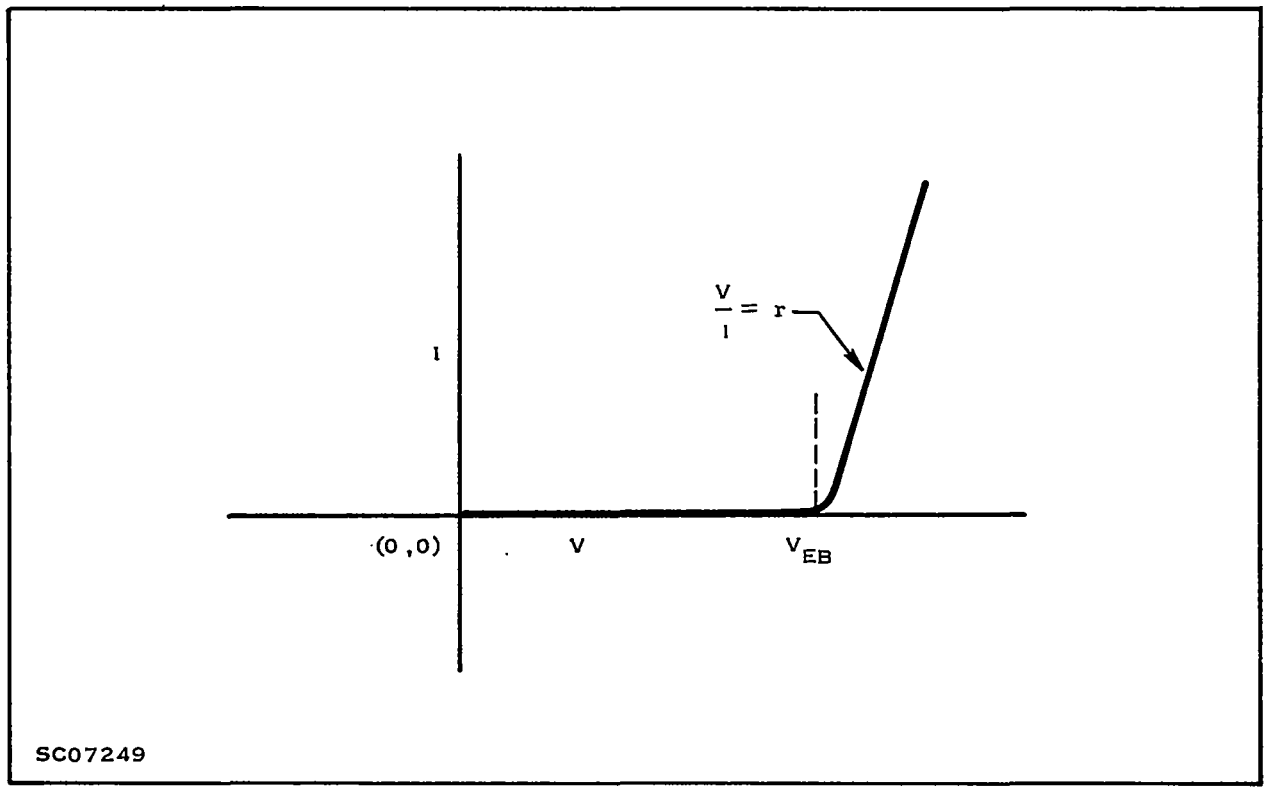

Figure 3-33. Expected Curve Tracer Display with "Plus" Polarity on Pin No. 7 of Circuit shown in Figure 3-29

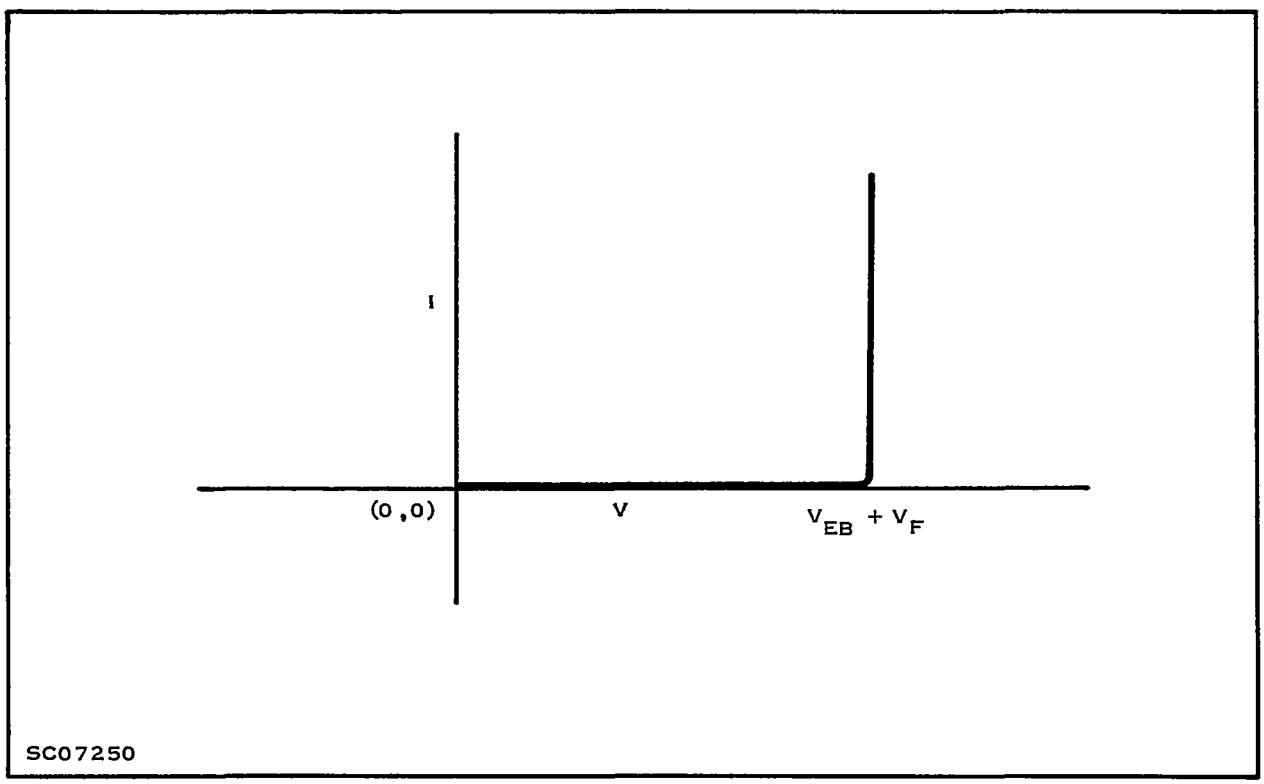

Figure 3-34. Expected Curve Tracer Display with "Plus" Polarity on Pin No. 7 of Circuit shown in Figure 3-32

pin 7 though the low-resistance substrate material ("P") and enter the resistor ("N") through that forward-biased P-N diode, and would flow out at pin 1. Thus, the actual trace obtained would be that of a forward-biased diode breakdown, as shown in Figure 3-35. Device design knowledge, combined with circuit design familiarity, are essential in the interpretation of the results obtained from pin-to-pin measurements using the curve tracer.

The preceeding example illustrated that pin-to-pin measurements are affected by subsurface or parasitic circuitry as well as the active circuitry of the device, and the expected trace characteristics are not always the actual trace obtained due to these parasitics.

One method of curve-tracer analysis is quite useful in that it compares the pin-to-pin traces of a questionable device with the identical traces of a good device. This comparison method requires little extra time. The method utilizes a test box that will accept two devices—one good, and one questionable or defective. Comparison of these two devices is made by means of a switch. One design for the test circuit is shown in Figure 3-36. The good device and the questionable device are both plugged into the box. The pin-to-pin measurement is selected by plugging curve-tracer leads into

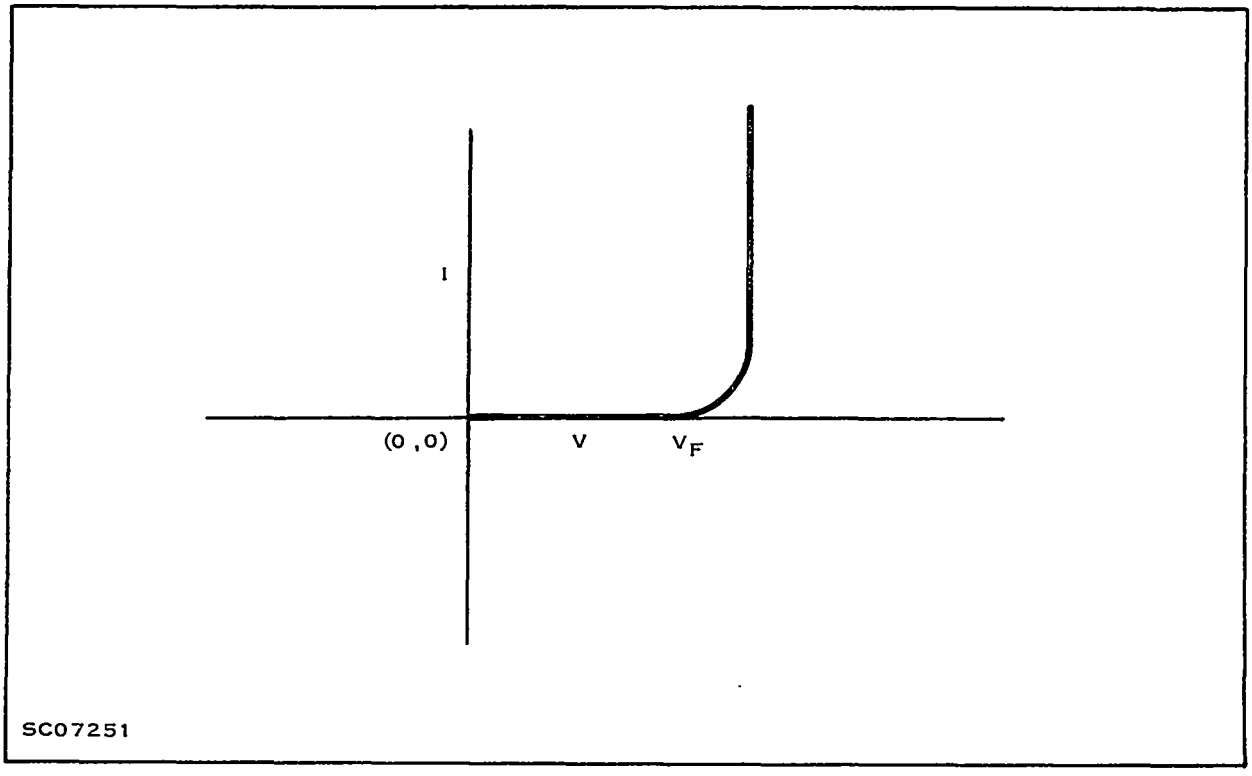

Figure 3-35. Actual Curve Tracer Display with "Plus" Polarity on Pin No. 7 of RCTL Gate

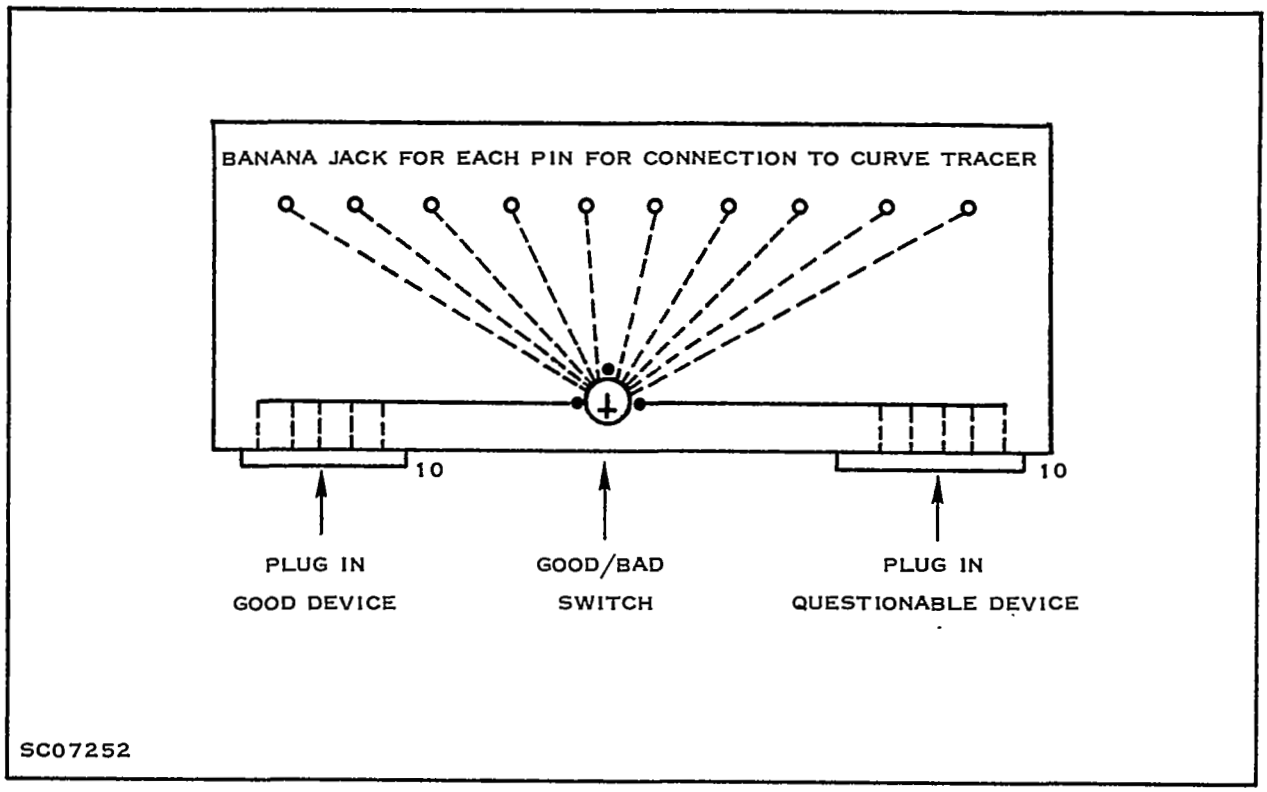

Figure 3-36. Test Box for Curve Tracer Comparison Testing

the appropriate lead jacks. The good-device trace is compared to the questionable-device trace by changing the position of the switch.

A "revised" circuit schematic should be useful to the analyst as an aid in the interpretation of curve traces which are affected by parasitic elements and circuit components constructed in a manner different from discrete components. Examples of such "revised" circuit diagrams will now be presented.

The circuit for a typical DTL gate is shown in Figure 3-37. This device is a triple diffused epitaxial device which utilizes a "P" type substrate and "N" type resistor isolation. The diffusion profile is shown in Figure 3-38. The transistor and coupling diodes are triple diffusions into a substrate for a four-layer component. The resistors and input diodes are two diffusions into a substrate, for a three-layer component. The substrate is biased to the lowest potential (ground) to obtain the reverse-bias isolation.

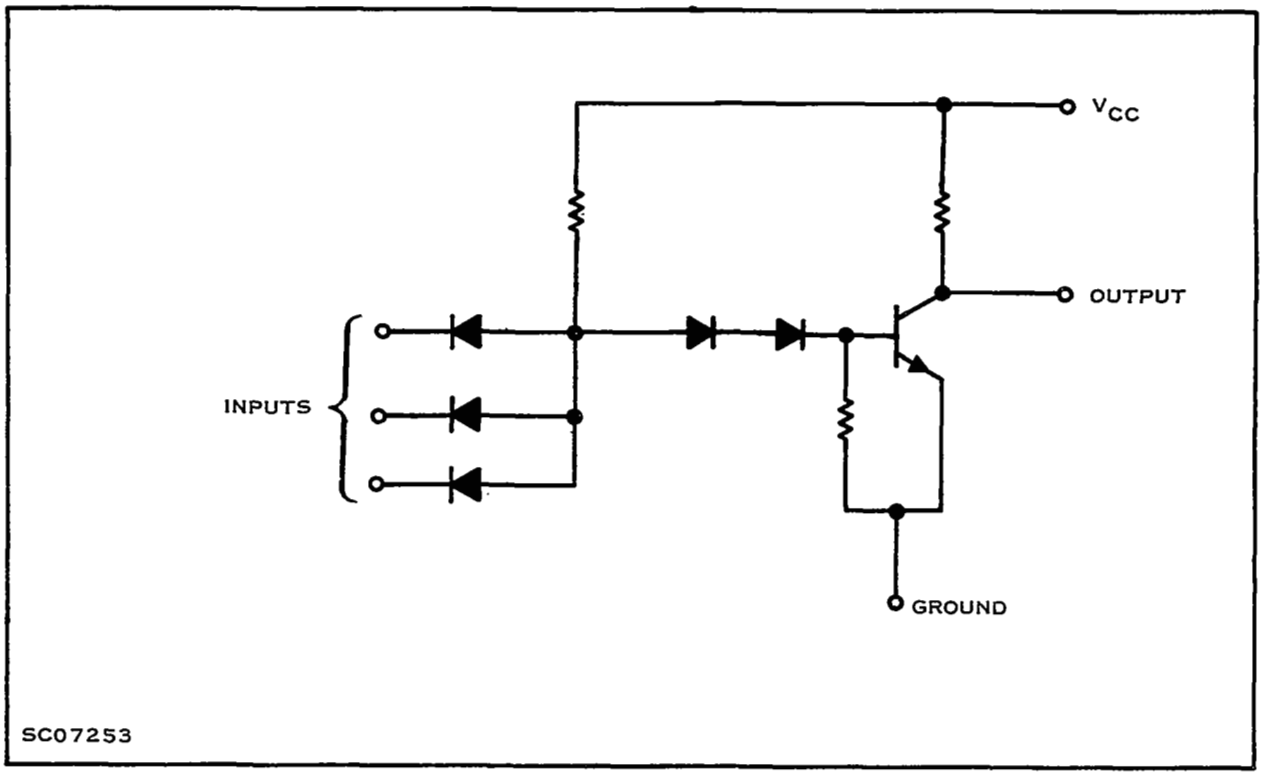

Figure 3-37. DTL Gate Circuit

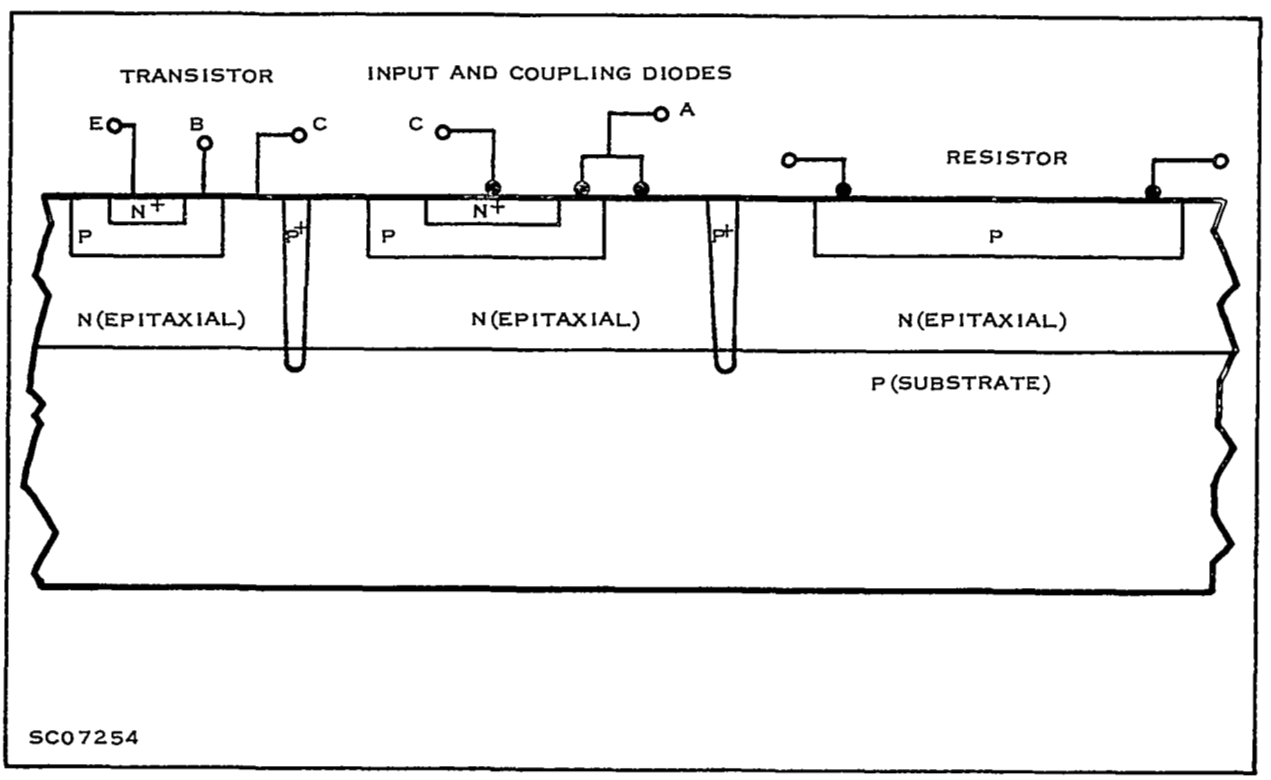

Figure 3-38. Diffusion Profile of DTL Gate

Each component of the circuit has been redrawn schematically in Figure 3-39 to include the parasitic elements that are present. Substituting these "revised" components into the circuit of Figure 37, the "revised" schematic diagram of Figure 3-40 is obtained. This "revised" schematic shows all current paths between pins, including the parasitic paths. Observation of the "revised" schematic will enable the analyst to determine which junctions or components can be observed by applying curve-tracer analysis or pin-to-pin measurements.

The circuit for a typical TTL gate is shown in Figure 3-41. The basic TTL gate uses the multiple-emitter input and the "totem pole" output concept and is a triple diffused epitaxial device using a "P" type substrate and "N" type resistor isolation. The diffusion profile is illustrated in Figure 3-42, showing the input transistor, the output transistor, the diode and the resistor diffusions. The substrate is biased at the lowest potential of the active circuitry (ground), and the resistor isolation is tied to the most positive potential (V_{CC}) to obtain the reverse-bias isolation effect common to monolithic microcircuits.

A study of the diffusion profile of Figure 3-42 permits the drawing of each component of the circuit schematically, including the parasitic elements of each component, as shown in Figure 3-43. Substituting these "revised" components into the circuit of Figure 3-41, the "revised" schematic diagram of 3-44 is obtained.

By using the comparison method and "revised" schematic diagrams, the analyst should be able to employ pin-to-pin measurements to narrow his search for a failure cause to an isolated portion of the microcircuit.

b. Linear Devices

Pin-to-pin measurements with the curve tracer when testing linear monolithic microcircuits differ only slightly from the measurements of digital microcircuits. An example of a linear circuit is an SN522 (Texas Instruments) operational amplifier that is capable of a nominal 60-dB open-loop voltage gain. A schematic of this device, including parasitic substrate diodes. is shown in Figure 3-45. The diffusion profile of the SN522 is shown in Figure 3-46.

A curve-tracer test, with plus on pin 2 and minus on pin 4, results in a forward-diode display because of the parasitic substrate diode. The same is true if pins 1, 6 or 8 are used in place of pin 2. Curve-tracer evaluation of the circuitry is difficult because of the large number of parallel parasitic elements.

Linear circuits utilizing dielectric isolation in place of reverse-biased P-N junctions may soon be in use. These will have far fewer parasitic elements.

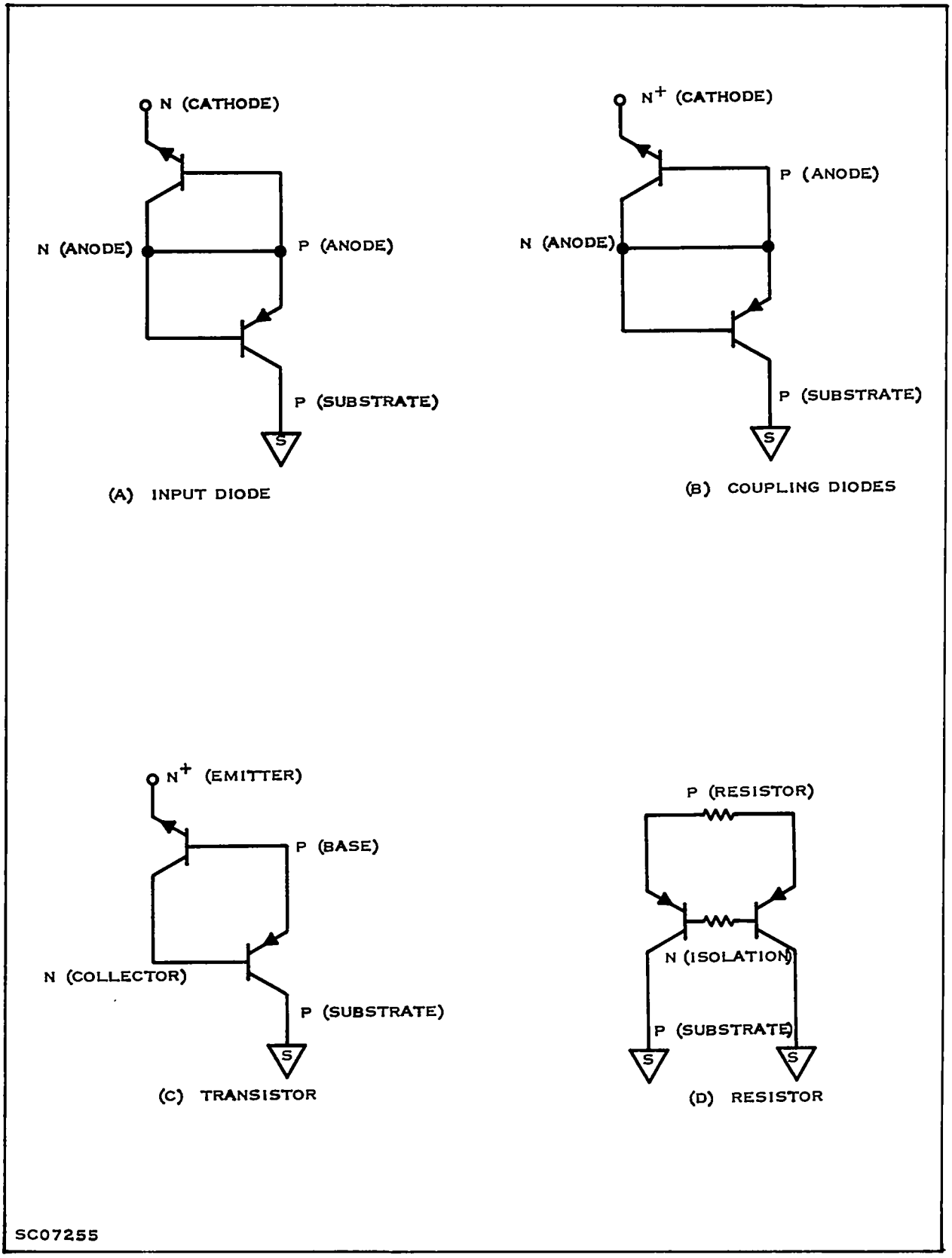

Figure 3-39. DTL Gate Circuit Components Showing Parasitic Elements

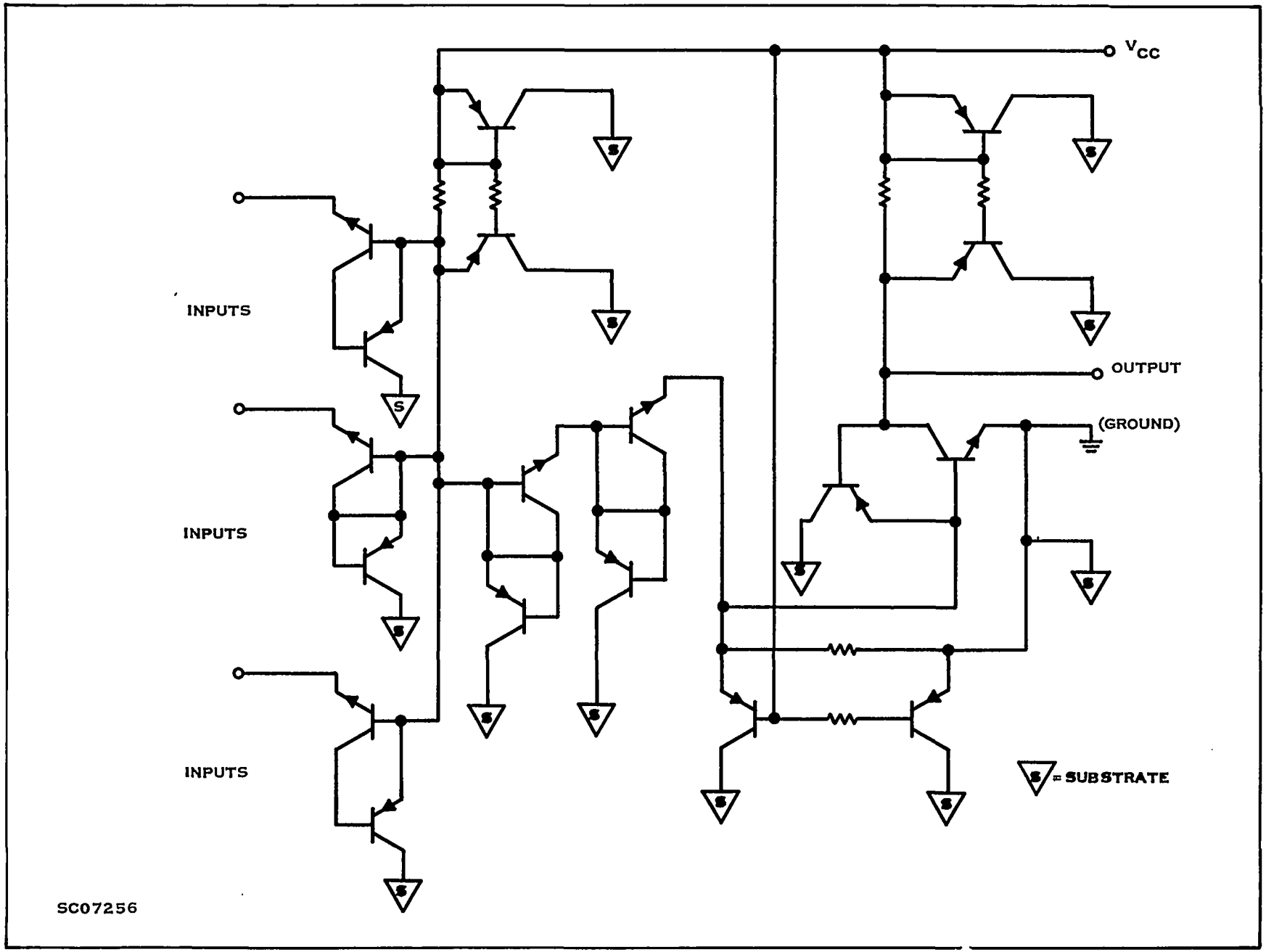

Figure 3-40. DTL Gate Circuit with Parasitic Elements Included

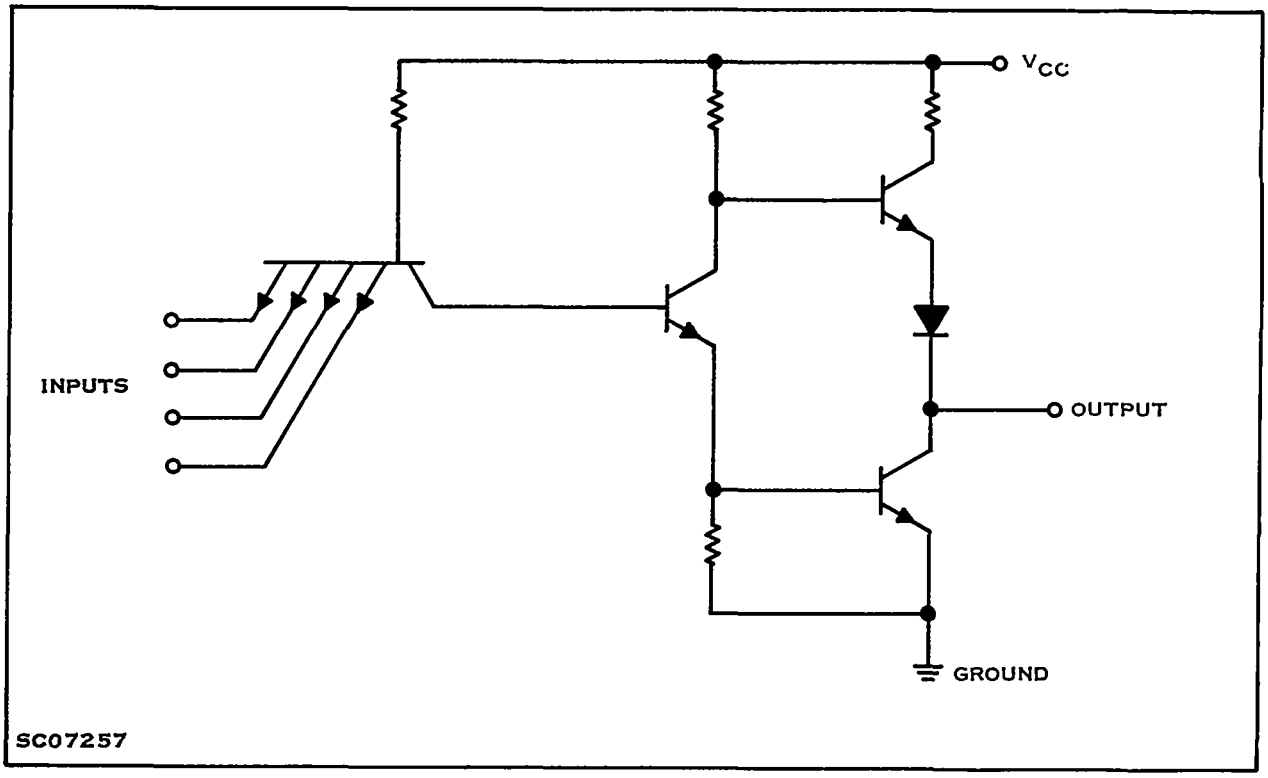

Figure 3-41. TTL Gate Circuit

D. MECHANICAL EVALUATION OF PACKAGE

1. Visual Evaluation Prior to Opening

When electrical tests have been completed, a complete visual evaluation of the package should be made. This evaluation may give valuable clues as to the cause of failure. Examine the device for missing or fractured external pins. If the device is in a test carrier, check for proper placement and orientation. Discoloration of the case may indicate excessive heating has occurred. Contamination on the case or terminals could cause leakage paths or resistive contacts. Dents in the case show improper handling, which may have resulted in shorted internal leads, a fractured bar or die, or hermetic seal leakage. Improper symbolization orientation may have caused improper terminal identification and mounting. Observe the position of the external pins in the glass eyelets. If a close proximity to the case is observed, closer inspection should be made with a microscope. The glass eyelets should also be observed. Cracks would indicate improper handling, and voids would identify a possible hermetic-seal leak. Finally, the cap weld should be observed for cracks that might permit a hermetic-seal leak.

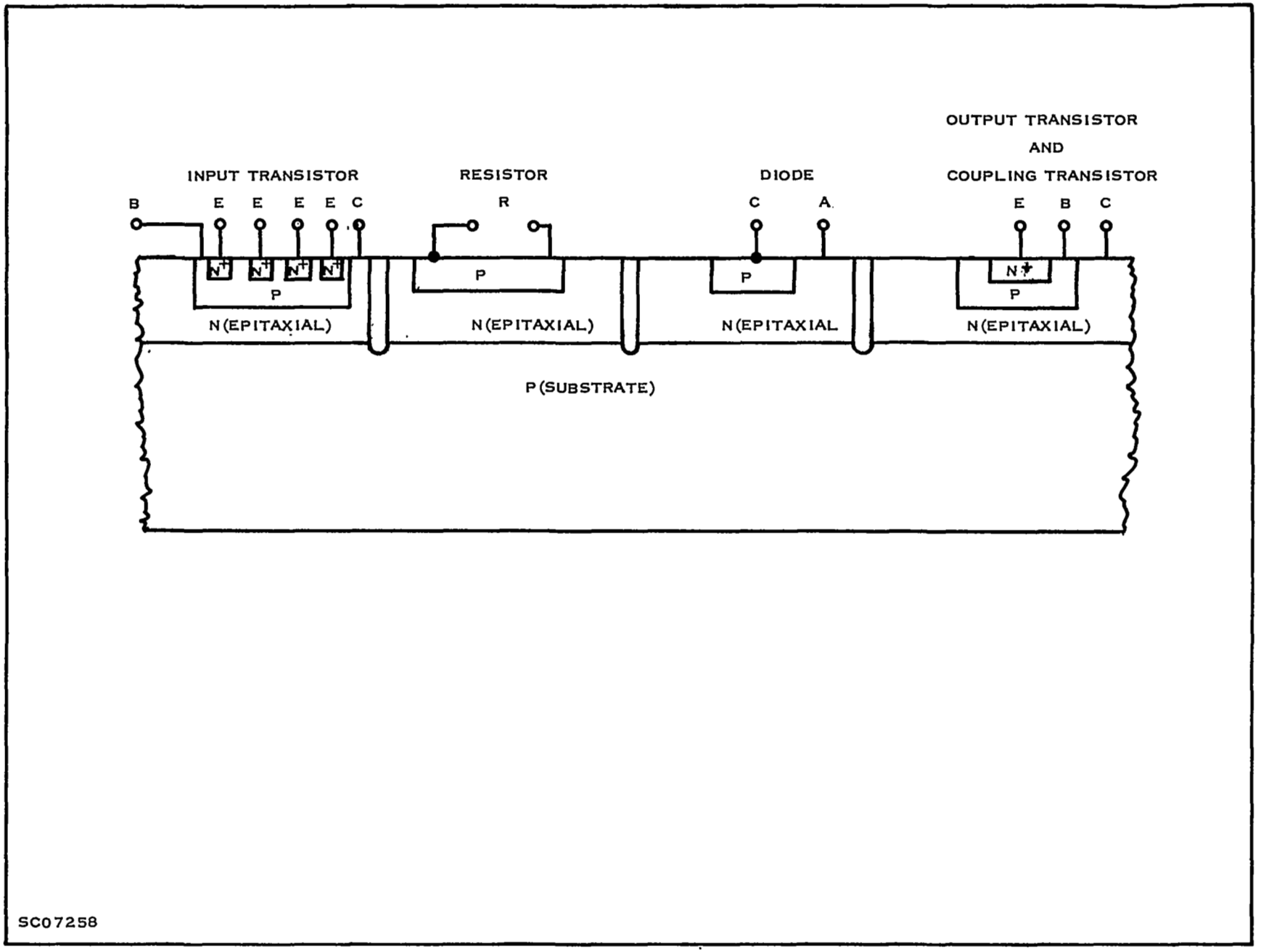

Figure 3-42. Diffusion Profile of TTL Gate

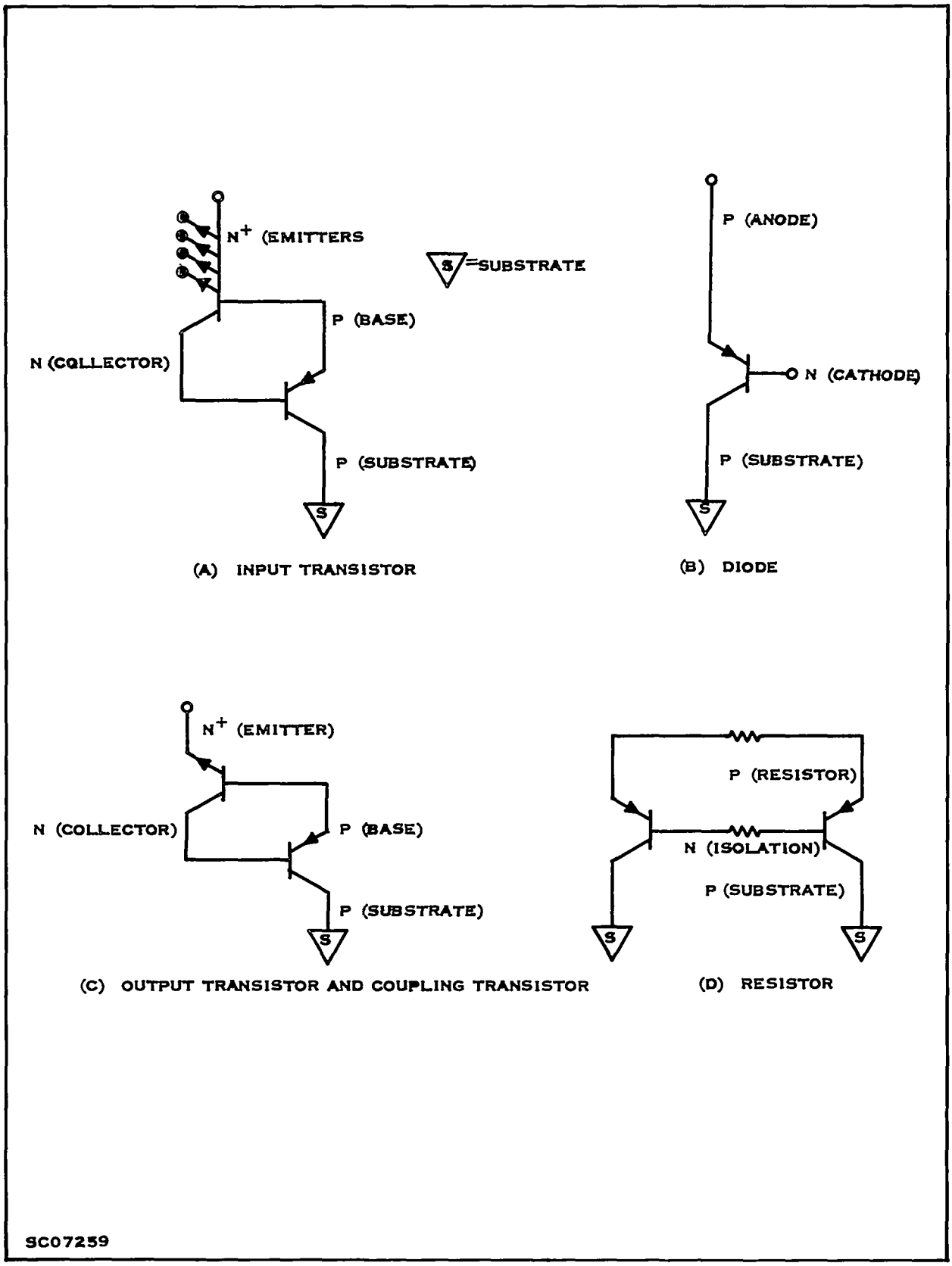

Figure 3-43. TTL Gate Circuit Components Showing Parasitic Elements

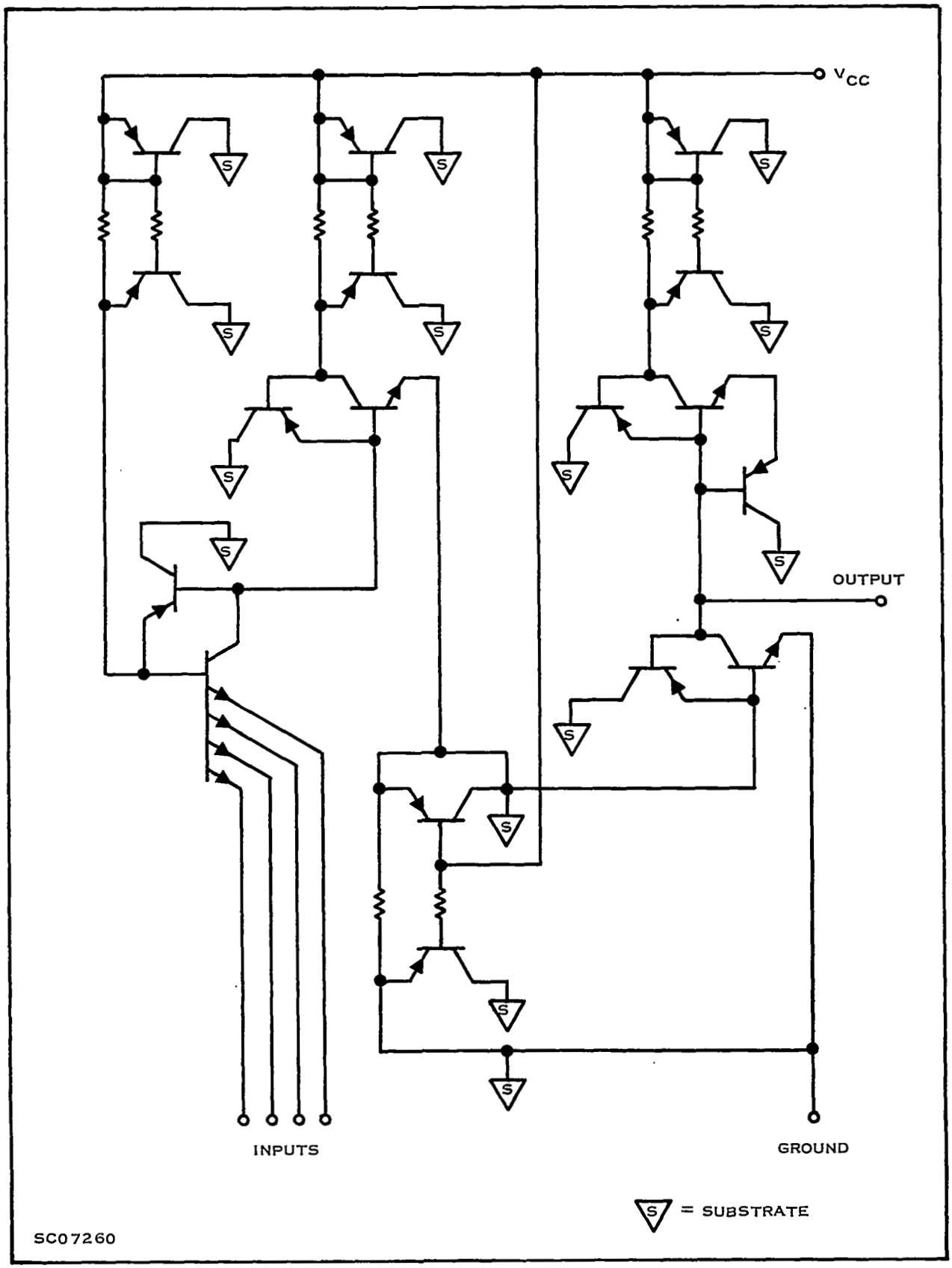

Figure 3-44. TTL Gate Circuit with Parasitic Elements Included

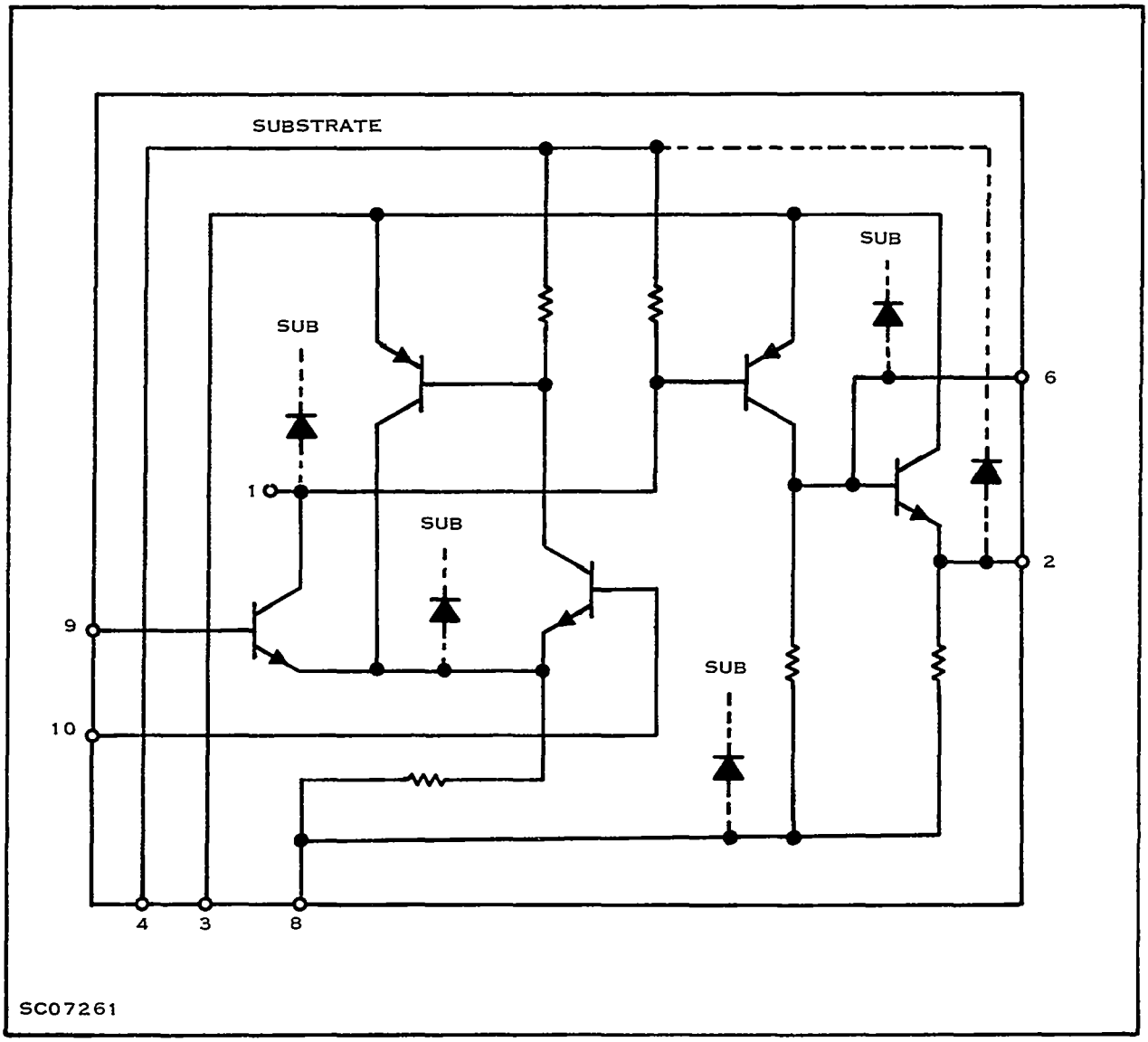

Figure 3-45. Schematic with Parasitic Elements shown in Dashed Lines

2. Radiographic Analysis

An X-ray or radiograph is a useful tool for the analyst. Normally, the top (plan) view of the device is the most useful view with which to observe most defects. A side view is desirable if certain failure modes are suspected, such as fractured pyroceramic or inadequate clearance between internal wires and case. Ideally, the device may be observed by making use of filmless radiography which utilizes a closed circuit television system to view the device while rotating it with a remote control device. A more three-dimensional effect is obtained in this manner. Radiographic analysis is useful to determine voiding in the pyroceramic or alloy (eutetic) mounting material beneath the bar or die, position and dress of internal wires before opening the device, the presence of pigtails and broken wires or

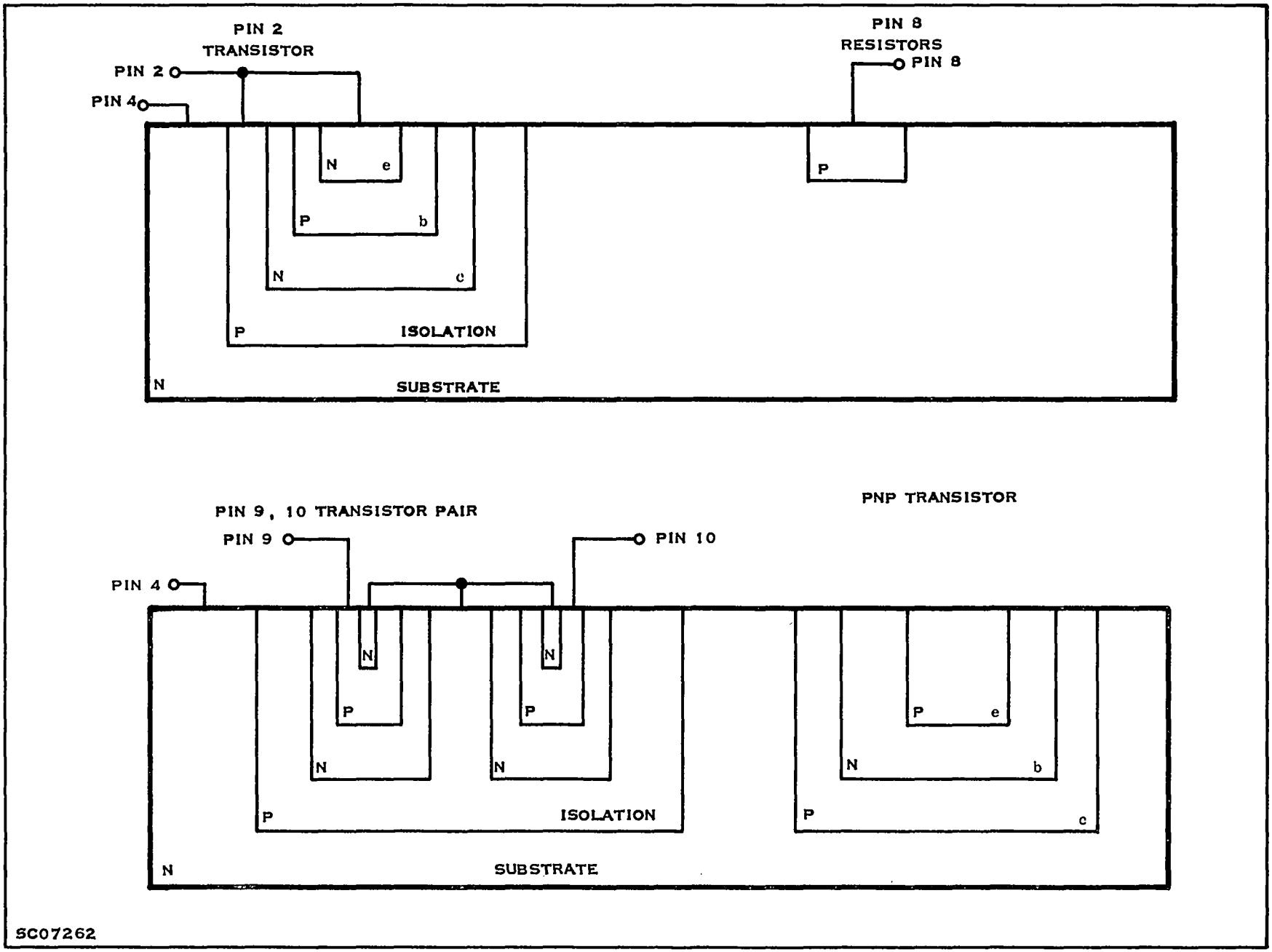

Figure 3-46. Diffusion Profile

extraneous material inside the package and the probable position of the bar or die within the package. It should be emphasized that radiographic examination is only an aid; it cannot take the place of careful visual examination after the device has been opened.

3. Hermeticity Evaluation

The final test to be made before opening the device is a hermeticity evaluation. Four primary means for performing hermeticity checks are useful to the analyst. Two of these may be used to detect "minor" leaks (less than 10^{-5} cm^3/s) and two may be used to detect "gross" leaks (greater than 10^{-5} cm^3/s).

One method for detection of "minor" hermetic-seal leak detection method employs helium. The device is placed in a high-pressure helium atmosphere (45 lbf/in^2) for approximately four hours. After removal from the helium atmosphere the device is placed in a mass spectrometer which measures the rate of helium "build-up." This rate is related to the leak rate of the hermetic seals.

The other "minor" leak detection method employs radioactive krypton. The device is placed in a high-pressure environment (44 lbf/in^2 or greater depending on package type) for approximately 0.2 hour. The length of time the device is left under pressure is determined by the leak rate to be tested and the lifetime and concentration of the radioactive material employed. After removal from this atmosphere, the device is placed in a counter equipped with a geiger tube. The radioactive disintegrations of any radioactive krypton that may have been forced into the device through any seal faults are measured through the case by the counter. This measurement is then related to the leak rate of the hermetic seals. This method of detection of "minor" leaks has an advantage over the use of helium in that the counter is capable of distinguishing between gas entrapped within the package and gas trapped externally by contamination, symbolization, or labels. It has the disadvantage of the possibility of radioactive contamination beyond that considered safe, resulting in inability to analyze the device until natural decay of radiation occurs. This, however, occurs very rarely. Neither the helium nor the radioactive krypton methods are capable of detecting "gross" hermetic seal leaks.

One "gross" leak-detection method employs hot (150°C) polyethylene glycol. The device is immersed in the polyethylene glycol and observed through a low-power microscope. A "gross" leak is determined by a steady stream of small bubbles. The source of the bubbles indicates the location of the leak. This test is not entirely satisfactory since the polyethylene glycol can enter the package through the defective seal and cause damage to the device. It does, however, take little time to perform and uses inexpensive equipment.

The second "gross" leak detection method employs alcohol at room temperature. In this test, the device is placed in an air atmosphere chamber at high-pressure (45 lbf/in^2) for 0.5 hours. After returning the device to ambient pressure, it is immersed in alcohol and observed through a low-power microscope. A steady stream of small bubbles again designates a "gross" hermetic-seal leak, and the location of the leak may be observed. The alcohol method, while requiring more time and equipment, is superior to the polyethylene glycol method because alcohol is a solvent for organic material which may have clogged a leak, and the alcohol is not harmful to the device if it enters the package.

Leak detection methods employing dye, which is inserted in the package, may be used. In this case, the dye has a very-low surface tension and seeps out through leaks in the hermetic seal. This method is not generally satisfactory because of the difficulty in inserting the dye without damaging the device, and further analysis is handicapped by the extreme difficulty in removing the dye from the interior of the package.

An example of a leak discovered by the "gross" leak polyethylene glycol method is shown in Figure 3-47. The leak is in the weld seal and is visible as a space between the lid and the ring frame. The leak test equipment is shown in Figure 3-48.

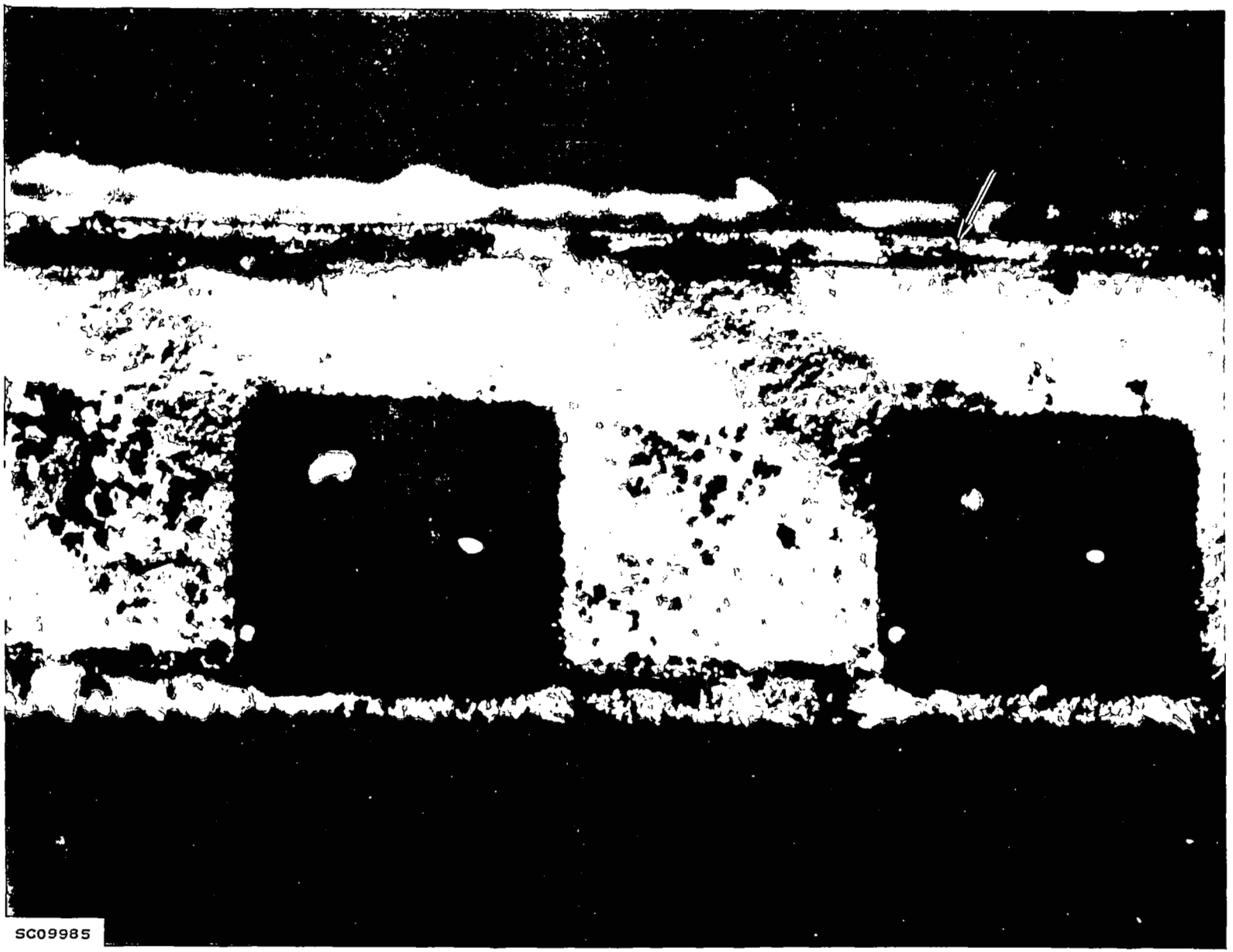

Figure 3-47. Weld-Seal Leak in Flat Pack, Found by "Gross" Leak Test Method

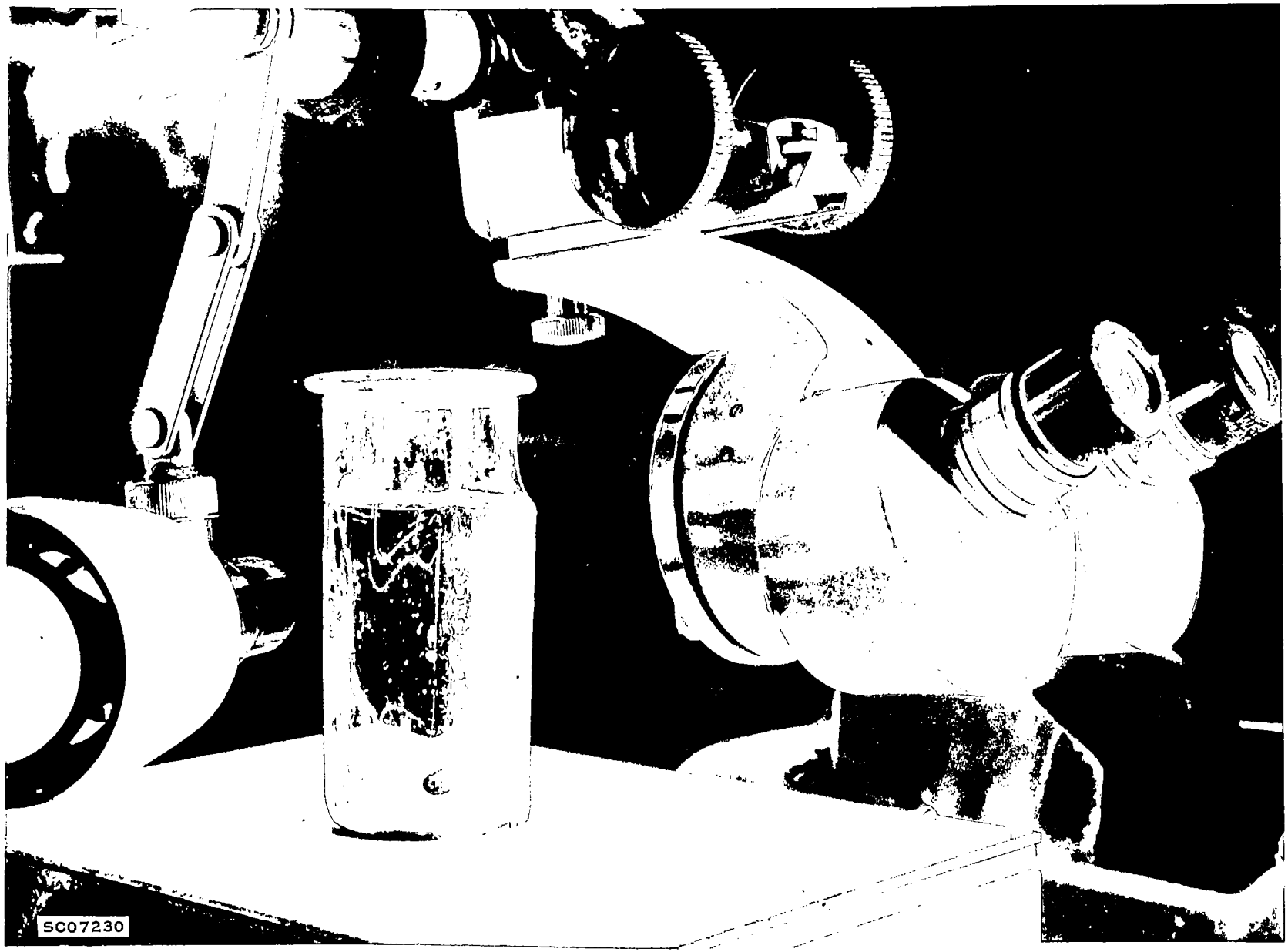

Figure 3-48. Polyethylene Glycol Gross-Leak Test Equipment

SECTION III

HOW TO OPEN THE PACKAGE

A. FLAT PACKS

1. General

The flat pack is manufactured in several different sizes, with a variety of materials. Those made of primarily metal, such as TO-84 and TO-89 (illustrated in Figure 3-49) may be opened by any one of the methods discussed in the next few paragraphs. Those with mainly ceramic or nonmetallic materials, such as TO-91 and TO-86, may be opened by using a sharp-edged instrument to pry the lid off following a 5- to 10-minute soak in boiling acetic acid to soften the adhesive used.

2. Micromilling Machine

One of the most rapid ways to open the metal flat-apck package is by making use of a micromilling machine. For photographs of a typical machine see Figures 3-50, 3-51, 3-52 and 3-53. This machine, which has a small electrically driven milling wheel and micromanipulators to move the device or milling wheel in the X, Y and Z planes, is used to mill a narrow groove around the periphery of the cap of the package. This groove should cut through the weld bead of the cap, thus freeing the cap from the case. Care must be taken that the milled groove is not too deep, or damage may occur to the glass eyelet material within the package or to other portions of the package. Likewise, care must be used so that the groove is not cut farther from the edge than the weld bead, or damage may occur to internal terminals, connecting wires, or the die itself. If properly used, the micromilling machine will open the package cleanly and smoothly, and the possibility of damage to the interior of the package will be remote.

The flat pack is held in place either by a vacuum system or a mechanical method. The vacuum method requires a cavity under and fully covered by the bottom of the package. A small amount of sealant applied to the bottom of the package contributes to a better vacuum. Packages without a flat bottom may require a small pressure on the lid to hold them in place while they are being opened.

The mechanical method can utilize a number of means to stabilize the package. One method clamps to the package beneath the leads. Another applies pressure to the top of the leads. This sometimes results in the breaking of leads. Although it has not been attempted, a method combining both vacuum and mechanical force might be very satisfactory.

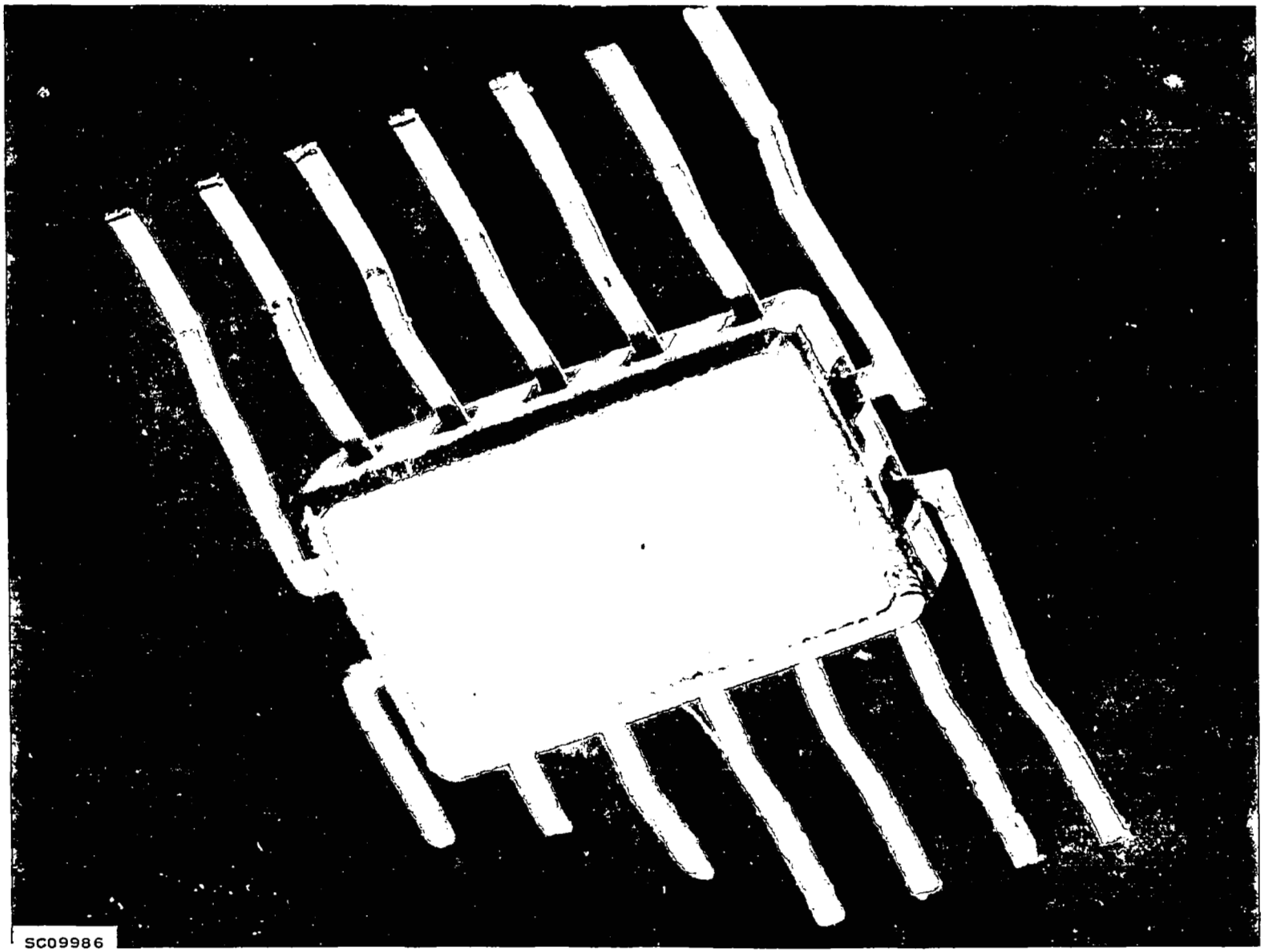

Figure 3-49. Type TO-84 Monolithic Microcircuit Flat Pack

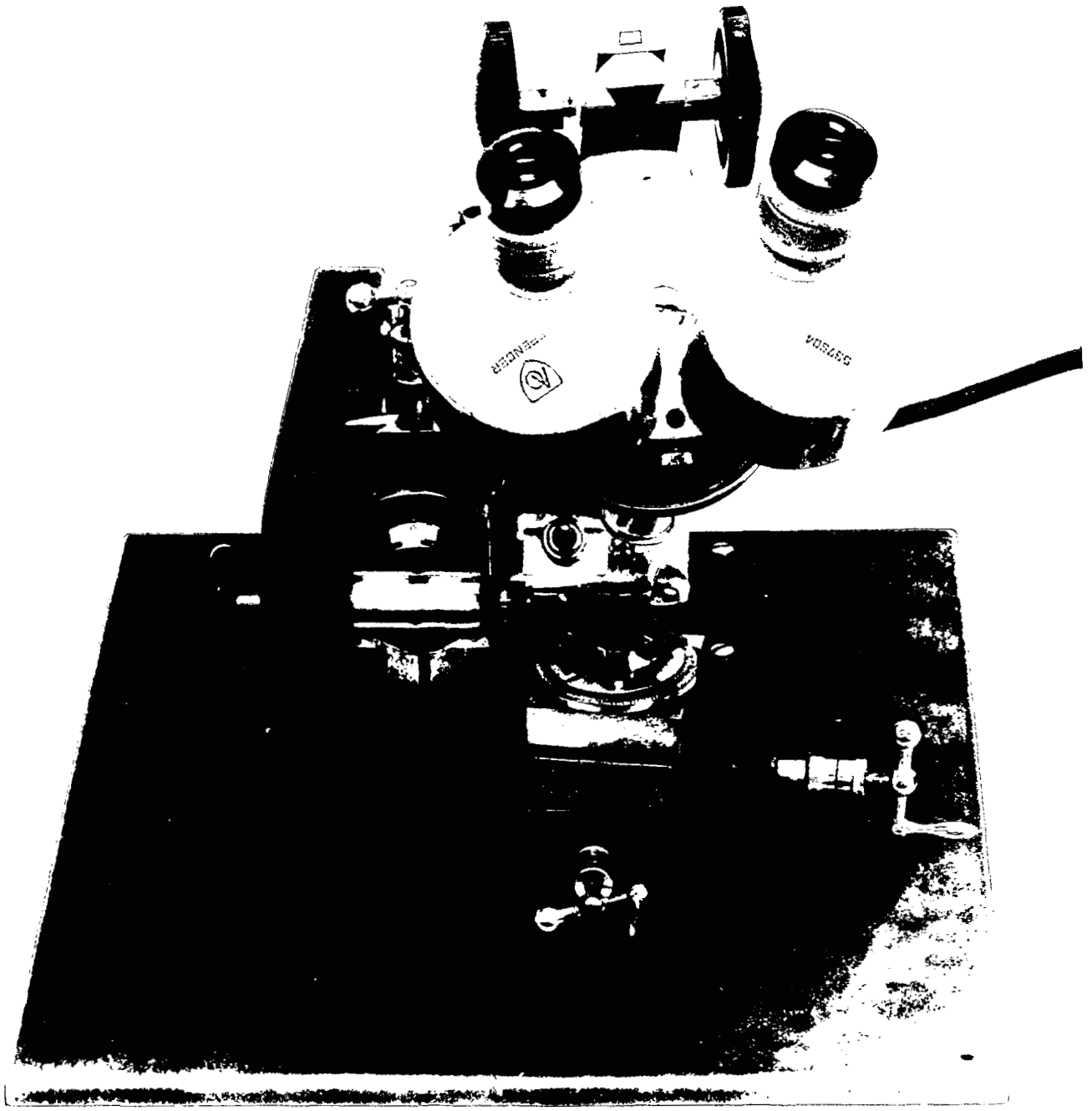

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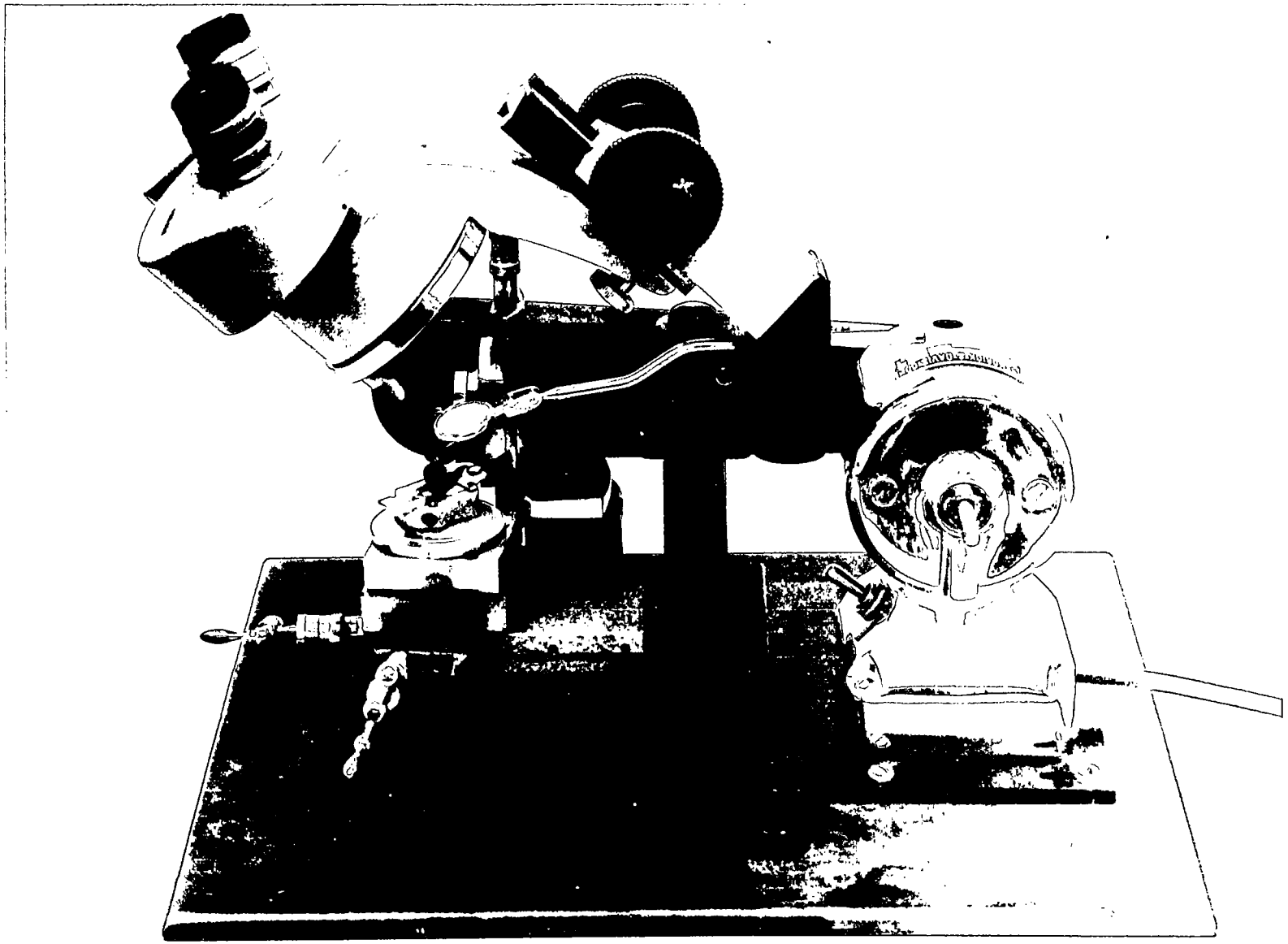
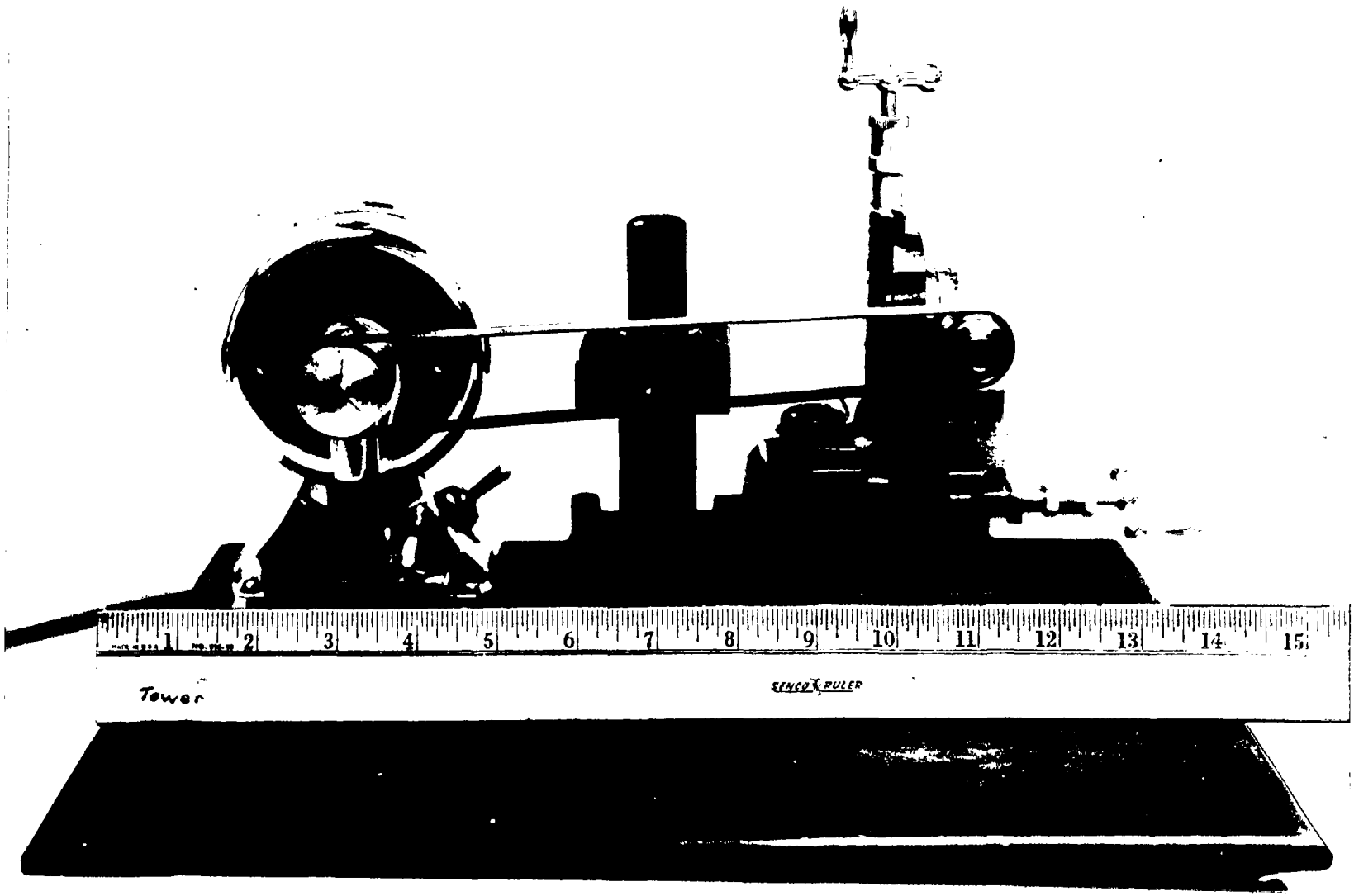
Figure 3-50. Micromilling Machine for Opening Metal Flat Packs



SC09988

Figure 3-51. Micromilling Machine for Opening Flat Packs



SC09989

Figure 3-52. Portion of Micromilling Machine for Opening Metal Flat Packs

Figure 3-53. Milling Wheel and Mechanical Hold-Down of Micromilling Machine for Opening Flat Packs

3. Knife or Sharp-Edged Instrument

One method of opening the package is by making use of a knife, or other sharp-edged instrument. The first requirement for opening the device in this manner is a fixture to hold the device firmly without damage to the package. This fixture must necessarily grip only the bottom portion of the flat pack, below the external terminals, to prevent damage to terminals and to give access to the cap of the package. With the flat pack held securely in the fixture, a knife is used to cut off the weld bead around the case of the package. After cutting the weld bead, the cap may be lifted from the flat pack. This method of opening the package necessarily places considerable stress on the package and often results in cracked glass and fractured dies (bars). External terminals also suffer damage unless great care is used. This method does have the advantage of using inexpensive equipment.

4. Sanding

The cap on a flat pack device may be removed by sanding. To accomplish this, the device must be mounted in a suitable fixture to hold it rigid, or it may be glued to a flat surface, using any substance that can be easily removed. If glue or a similar substance is used, care must be taken in removing the device so that undue stress is not placed on the package. The device may be held while the cap is sanded off by hand, or a fine grit grinding disc may be used. Sanding should be done as evenly as possible to insure ease of removal of all of the cap from the case. This method of opening the package has the advantages of using inexpensive equipment, and it is reasonably rapid. It has the disadvantages of possible heating of the device from the sanding, almost certain damage to external terminals, and the introduction of foreign particles into the package.

B. IN-LINE PACKAGES

In-line packages of various materials are available on the market. The bulk of the package is generally of a ceramic or epoxy material. Two general classifications exist: 1) an open, hermetically sealed space surrounds the top portion of the bar, 2) no open space exists.

The package containing an open space may have a metal lid which can be milled off at the edges. Nonmetallic lids which are also used can be pried or sanded off or pried off following a 5- to 10-minute soak in boiling acetic acid to soften the adhesive used. Care must be taken to avoid damaging the bar and connecting wires.

Those packages without open space over the bar must be attacked carefully to avoid destroying valuable evidence. A typical example of such a package is shown in Figure 3-54. After a thorough electrical analysis has been made, one method

SC09991

Figure 3-54. Plastic In-Line Package

of gaining access to the bar is to remove most of the material above the bar by sanding or sectioning. At some point before reaching the bar surface, the wires connecting the bar to the external leads will be encountered. At that time it is advisable to perform some electrical tests if any open circuits are suspected. A continuity test from the connecting wire to the external pin will evaluate that portion of the circuit. Continued removal of material by sanding is then required to reach the bar. Some units have a transparent material in the immediate vicinity of the bar. If this is the case, visual examination of the bar surface may reveal usable information.

In many cases, access to the surface of the bar is required in order to perform probing, lead removal and, when nontransparent material is used, visual inspection.

Removal of the material over the bar may be accomplished by placing the device in heated epoxy strip for a short period of time, five to ten minutes in most cases. This treatment will loosen or completely remove the material over the bar. If only loosening occurs, tweezers may be used for complete removal. Epoxy strip may attack aluminum leads somewhat if the time of application is excessive. Epoxy strippers are available from several manufacturers. Sulfuric acid heated to the fuming point for 10 minutes may be substituted for the epoxy strip.

Disadvantages of this method of gaining access to the bar of the in-line package are 1) considerable time is required, and 2) some of the ball bonds are likely to be pulled away as the material is removed. An alternate method which does not endanger the ball bonds has not been developed.

CAUTION

Sulfuric acid will remove aluminum if not fumed sufficiently or if application is excessive.

C. TO-5 PACKAGES

The method of opening a TO-5 package is the same, regardless of the contents. Microcircuits are mounted in modified TO-5 cans that contain more pins than do transistor cans. In either case, the commonly used method is to remove a small amount of metal from the full circumference of the base of the can. The depth of metal to be removed is approximately equal to the thickness of the can material. Once the metal is removed, the top of the can may be detached with the fingers.

A typical package is shown in Figure 3-55. The method of metal removal is illustrated in Figure 3-56. The TO-5 can is first placed in a small chuck. The chuck-supported can is then moved in contact with a rotating resin-bonded silicon carbide disc. A 1725-rpm motor is the power source for the disc. The outside diameter of the disc is 4 in., and the inside diameter is 1/2 in. Either a 10- or 20-mil thickness may be used. Rotation of the can while maintaining contact with the disc results in the required metal removal. A protective shield over the disc prevents injury to the operator in case of disc breakage.

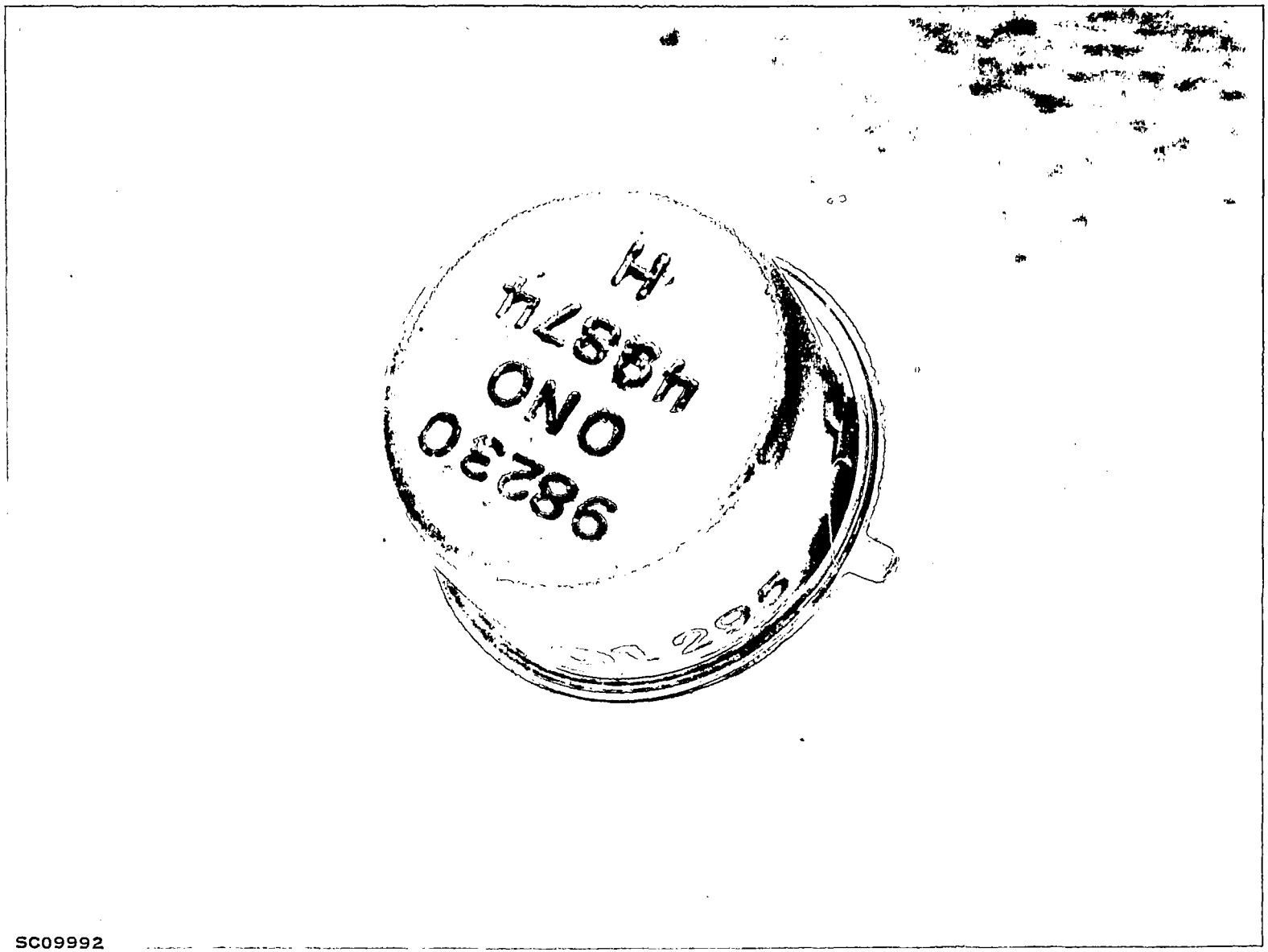


Figure 3-55. Modified Type TO-5 Package for Monolithic Microcircuits

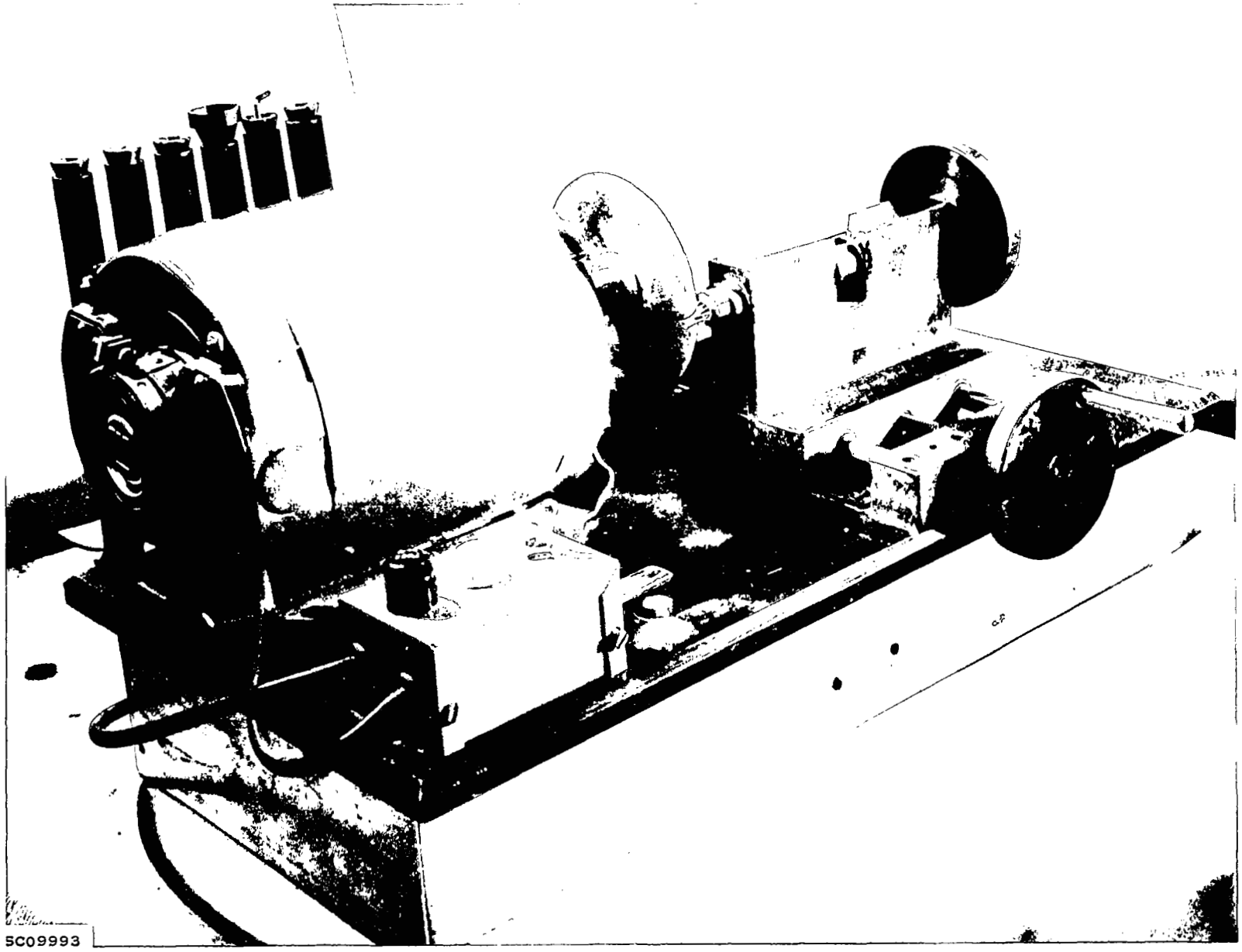


Figure 3-56. Decanner for Type TO-5 Package

SECTION IV

EVALUATION OF MONOLITHIC MICROCIRCUIT AFTER OPENING OF PACKAGE

A. GENERAL

Prior to opening the microcircuit package, certain information will have been learned about its condition. This information falls largely in the electrical area, since it has to do with parameter measurements, curve tracer tests, etc. The objective of opening the device is to determine what is causing the abnormal electrical characteristics or what could have caused those which no longer exist. The first step after opening is a visual inspection to locate any obvious defects which may exist. Observed defects must be evaluated to determine if they could cause the abnormal electrical characteristics. Occasionally a defect is noted which appears quite serious but in fact does not impair the device operation. The analyst must continually be on the alert for such deceptive conditions. Certainly a defect of serious appearance is not to be condoned even if it does not affect device operation. The point is that the analyst should not allow such a defect to cloud his search for the actual cause of failure.

After visual inspection is completed, further electrical evaluation will normally be required to investigate those defects observed visually or to obtain more information where visual observations were not fruitful. Chemical analysis may be required in some cases where unknown materials need to be identified. Visual, electrical and chemical evaluations are discussed in detail hereafter.

B. VISUAL INSPECTION

1. Equipment Required

The first evaluation to be made after opening the device is a thorough visual examination. In general, two types of microscopes are required to perform this examination. A stereo microscope of relatively low power (20X to 60X, preferably variable over this range), with diffused or oblique lighting is desirable when inspecting for mechanical faults, improper routing of connecting wires, misalignment of the die (bar) in the package and possible shorts of the internal pins. This same microscope may be used in subsequent analysis of the device.

For a close examination of the surface of the active element, a high-power metallurgical microscope with direct lighting is required. Assorted lenses should be available for this microscope to give a range of magnification from 35X to 400X. With this microscope, metallization faults, oxide defects, masking defects and improper diffusions may be observed. It is desirable that camera accessories be available for use with this microscope to photograph observed defects before disturbing the device to verify those defects. This microscope and camera will also likely be used in subsequent analysis of the device after the initial visual inspection.

2. Typical Examples of Problems

a. General

The following examples illustrate certain conditions which are frequently observed and/or discovered by means of a visual inspection of the microcircuit. The conditions are depicted with photographs, and the probable causes of the problems are discussed. For convenience the conditions are grouped in the following six categories:

- Process problems
- Evaporated leads
- Die problems
- Connecting wires
- External terminals
- Electrical overstress

b. Process Problems

(1). Photolithographic Mask Defect or KMER Defect. The photolithographic masking defect or KMER defect shown in Figure 3-57 resulted in an emitter diffusion into the base contact region, thus causing an emitter-to-base short of the transistor. It is virtually impossible to distinguish between a KMER defect and a photolithographic mask defect. These defects may appear at any place on a die, and in many different forms. The most common defects result in diffusions in improper areas, no diffusions in areas where there should be, oxide defects, and excess removal or nonremoval of metallization. The defects may be caused by incomplete coverage by the KMER, scratching or smearing of the KMER in handling, defective photolithographic masks, foreign material, or improperly handled masks. Depending on the type of defect, detection may occur in threshold tests, pin-to-pin tests, or parameter analysis.

(2). Faulty Metallization. Faulty metallization in the form of an open evaporated lead, and smaller areas lacking metallization are shown in Figure 3-58. This defect could be detected in threshold or pin-to-pin tests. The defect could have been caused by KMER or photolithographic mask defects, or by a faulty metallization removal process. The residue on the capacitor in the photograph would indicate that the latter was probably the cause.

(3). Excess Metallization. Excess metallization is shown in Figure 3-59. This example illustrates the shorting of components by metallization that was not removed from the die surface. Detection would occur during curve-tracer threshold, pin-to-pin measurements or parameter analysis. This defect is the result of a KMER or photolithographic mask defect which prevented the removal of metallization in this area.

(4). Metallization-Silicon Eutectic Formation. Metallization-silicon eutectic formation is shown in Figure 3-60. This illustration of a gold-silicon eutetic formation is typical of the visual indicator that is seen when the eutectic point has been reached. In this case, the gold ball bond and the bare silicon have formed the gold-silicon eutectic, i.e., the temperature (377°C) at which gold alloys into the silicon has been exceeded. This formation will normally be observed only at contact windows, since considerable time is required for the alloying to penetrate the oxide. The resulting short-circuit would be detected in curve-tracer threshold or pin-to-pin analysis. Open circuits are also common due to the excessive current flow and would be detected in the same tests. The usual cause for the metallization-silicon eutectic is electrical overstress or excessive heating.

(5). Oxide Defect. The defect in the oxide shown in Figure 3-61 was covered by an evaporated lead. The defect allowed the lead to contact bare silicon, resulting in a short to substrate. While the entire discolored area is not bare silicon, it indicates the top layer or layers of oxide were not existent. Numerous small areas of bare silicon show through the oxide that is present. Oxide defects may show up in curve-tracer threshold or pin-to-pin measurements, but usually, parameter analysis is required to locate the smaller defects. Defects of this type may be of an intermittent nature. Oxide defects may be caused by KMER or mask defects, improper etching, contamination or improper handling. Voltage in excess of normal operating values may also lead to oxide defect formation by inducing localized dielectric breakdown.

c. Evaporated Leads

(1). Evaporated Lead Open Because of a Scratch. This defect, an evaporated lead open because of a scratch, as shown in Figure 3-62, would likely be detected in threshold or pin-to-pin tests, depending on the location. This deep scratch, along with the other scratches on the evaporated lead, indicates poor workmanship which was probably caused by handling with tweezers. This type of failure can be time-dependent, with the reduced cross section of a scratched lead becoming an open circuit on a very slight electrical overstress.

Figure 3-57. Emitter-Base Short due to Mask Defect

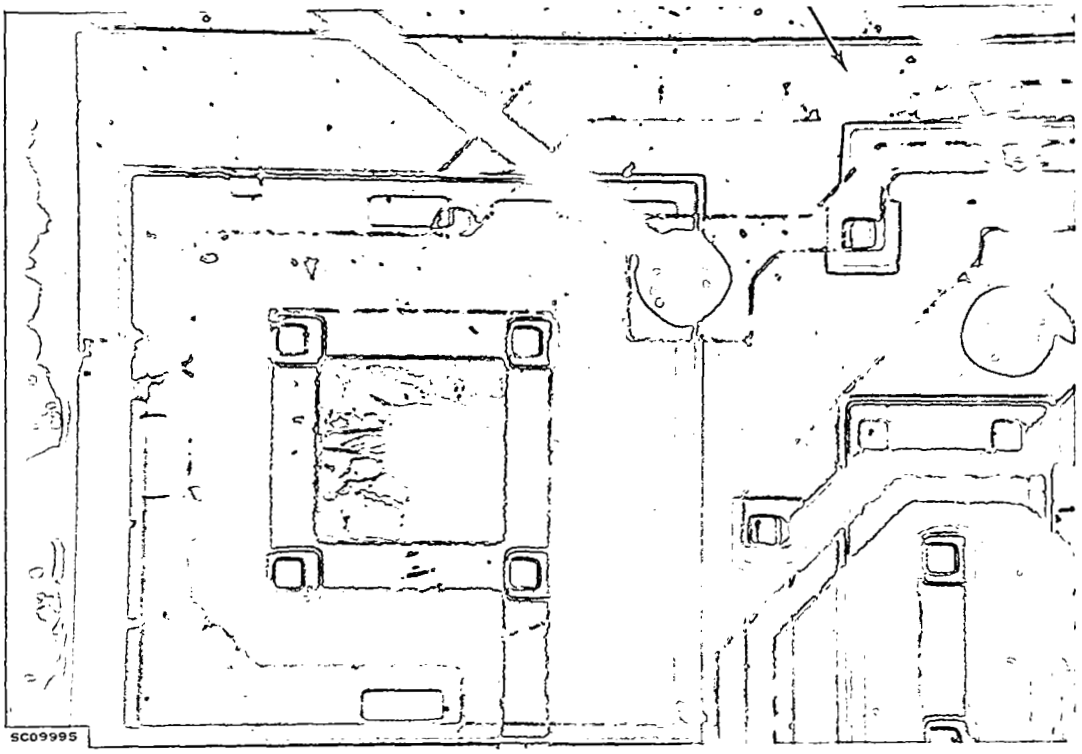


Figure 3-58. Open due to Faulty Metallization

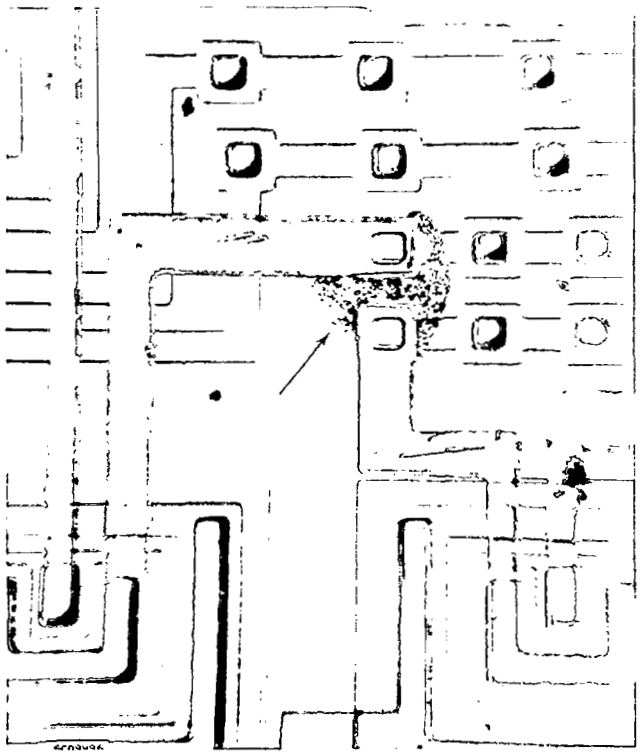


Figure 3-59. Short due to Excess Metallization

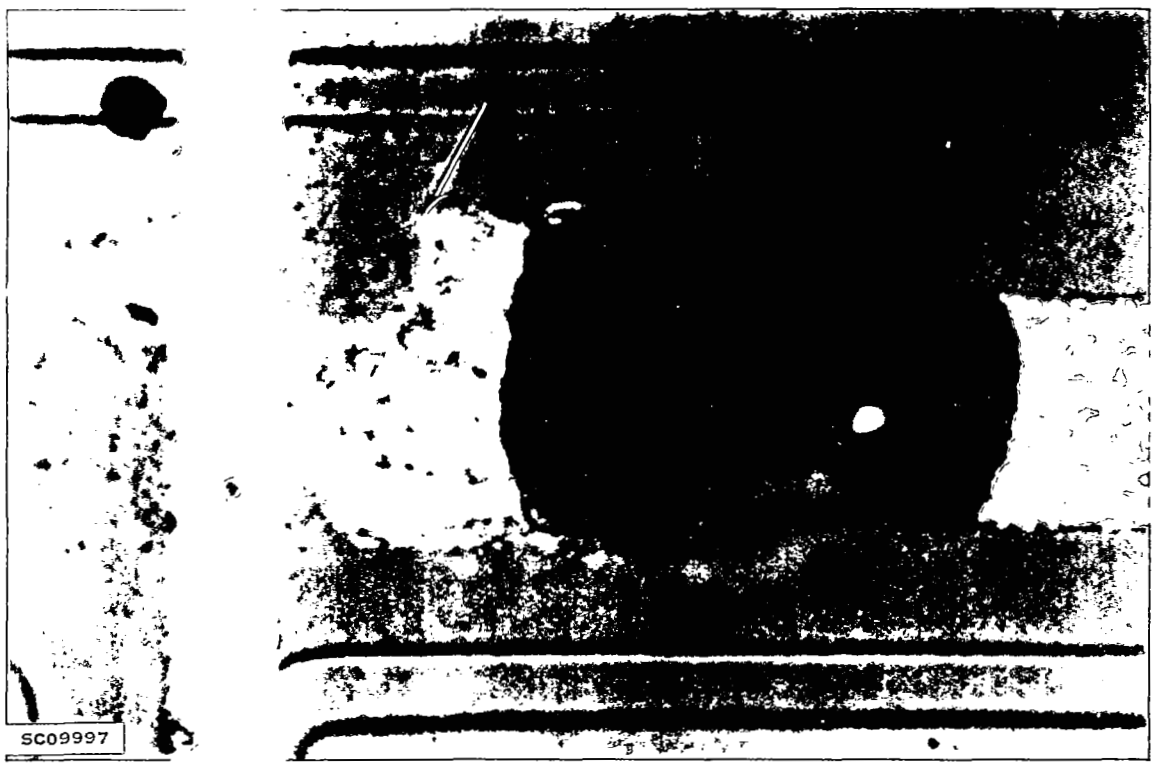


Figure 3-60. Gold-Silicon Eutectic

Figure 3-61. Oxide Defect Causing Lead-to-Substrate Short

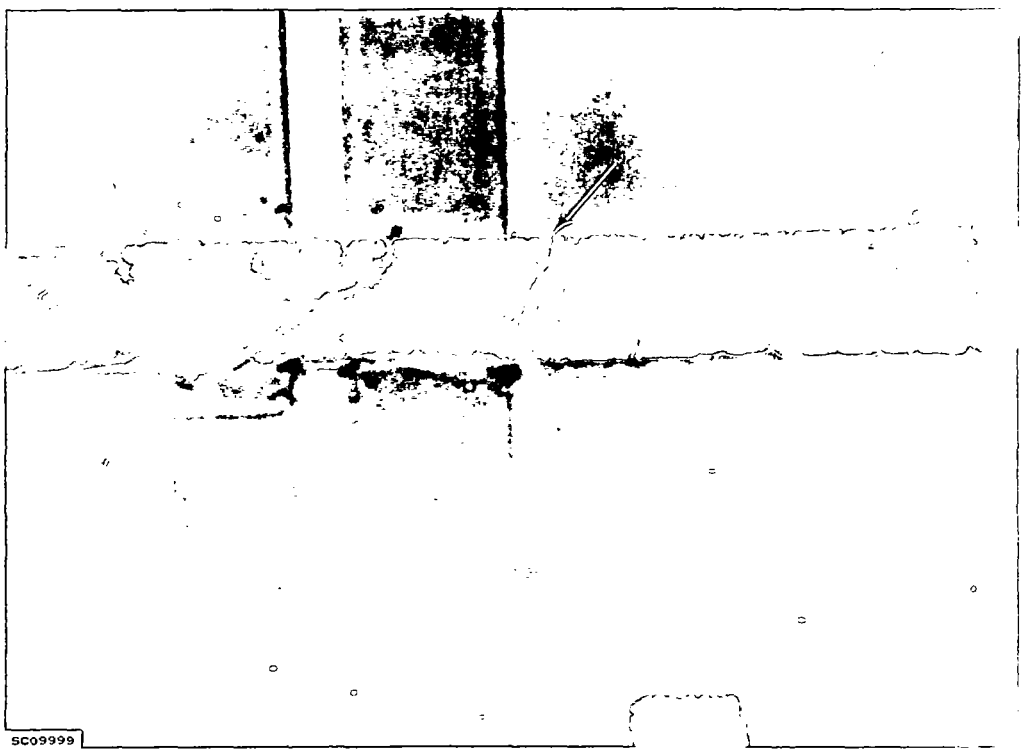


Figure 3-62. Open Lead due to a Scratch

(2). Smeared Evaporated Lead Pattern. The smeared evaporated leads shown in this photograph, Figure 3-63, were shorted together by the smeared gold. A portion of the bridging smear had been removed prior to taking the photograph. This defect would be discovered in the curve-tracer threshold test or pin-to-pin measurements. The smear could have been made in handling, bonding or probing operations.

(3). Separation of Bond from Evaporated Lead. Separation of a bond from an evaporated lead is illustrated by Figure 3-64. The raised ball bond shown in this example would be detected as an open circuit in preliminary threshold tests. The ball bond is observed to be flattened, indicating sufficient bonding pressure, but the bonding pad indicates only a small area of the bond adhered to the evaporated lead. Therefore, the likely cause of failure would be insufficient bonding temperature or bond-capillary dwell time.

(4). Chemical Reaction Between Evaporated Leads and Reagent Residue. Chemical reaction between evaporated leads and reagent residue will be described with reference to Figure 3-65. The illustration shows that an open circuit was caused by some of the evaporated leads having undergone a chemical reaction with a residue that was apparently left on the bar. The fact that only certain of the leads were attacked while adjacent leads were undamaged indicates that perhaps a galvanic action occurred. This defect would be detected in threshold and pin-to-pin tests. The possibility of moisture in the package contributing to the reaction should not be overlooked.

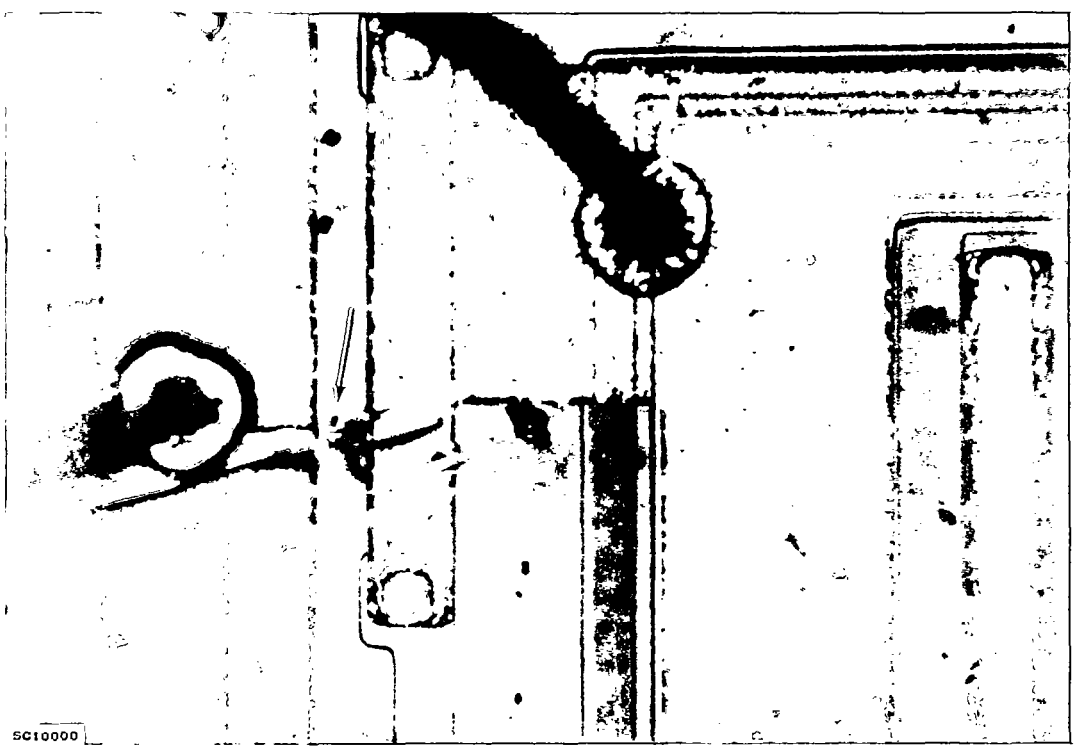


Figure 3-63. Short due to Smeared Leads

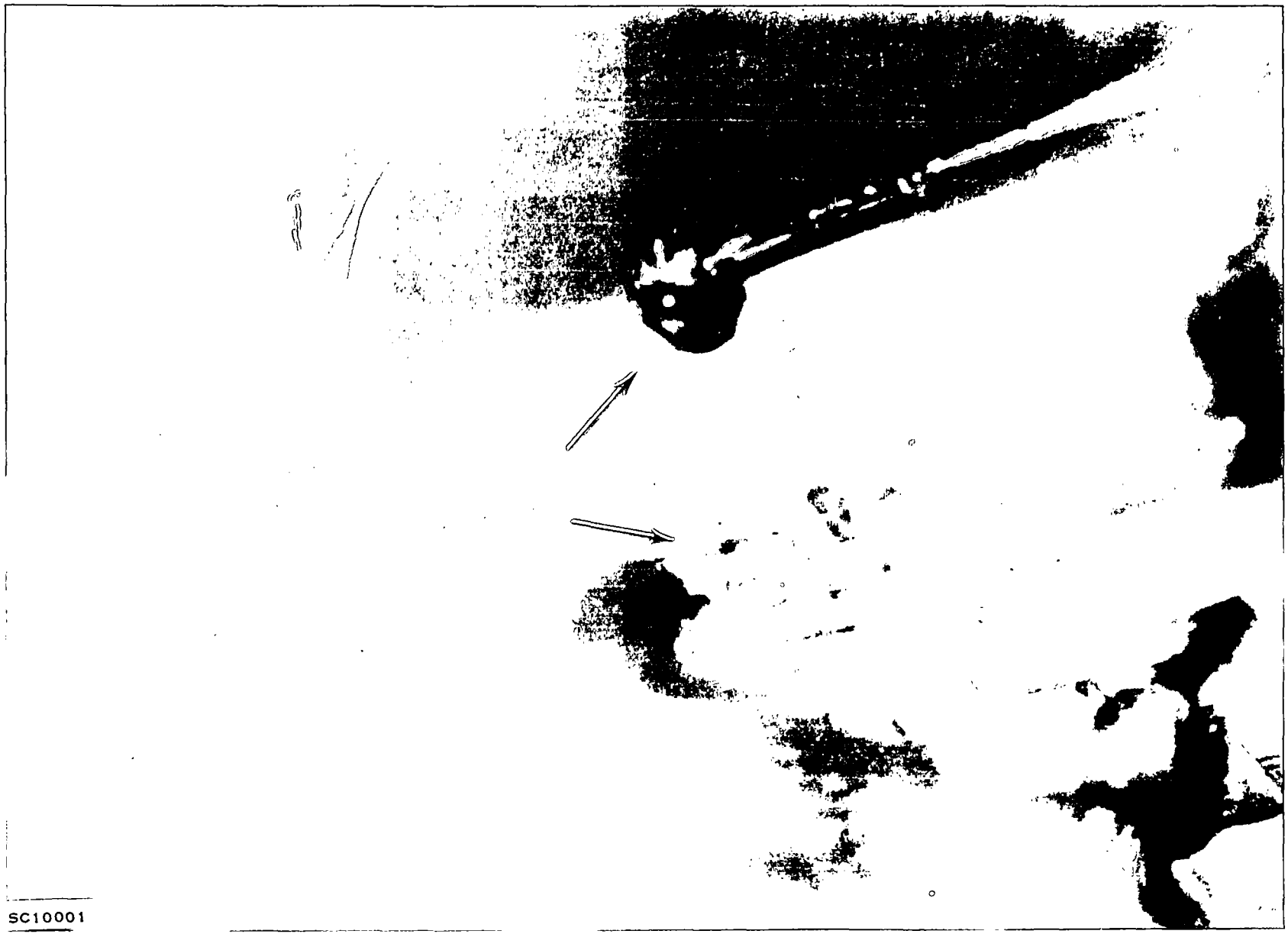


Figure 3-64. Ball Bond Separated from Bond Pad

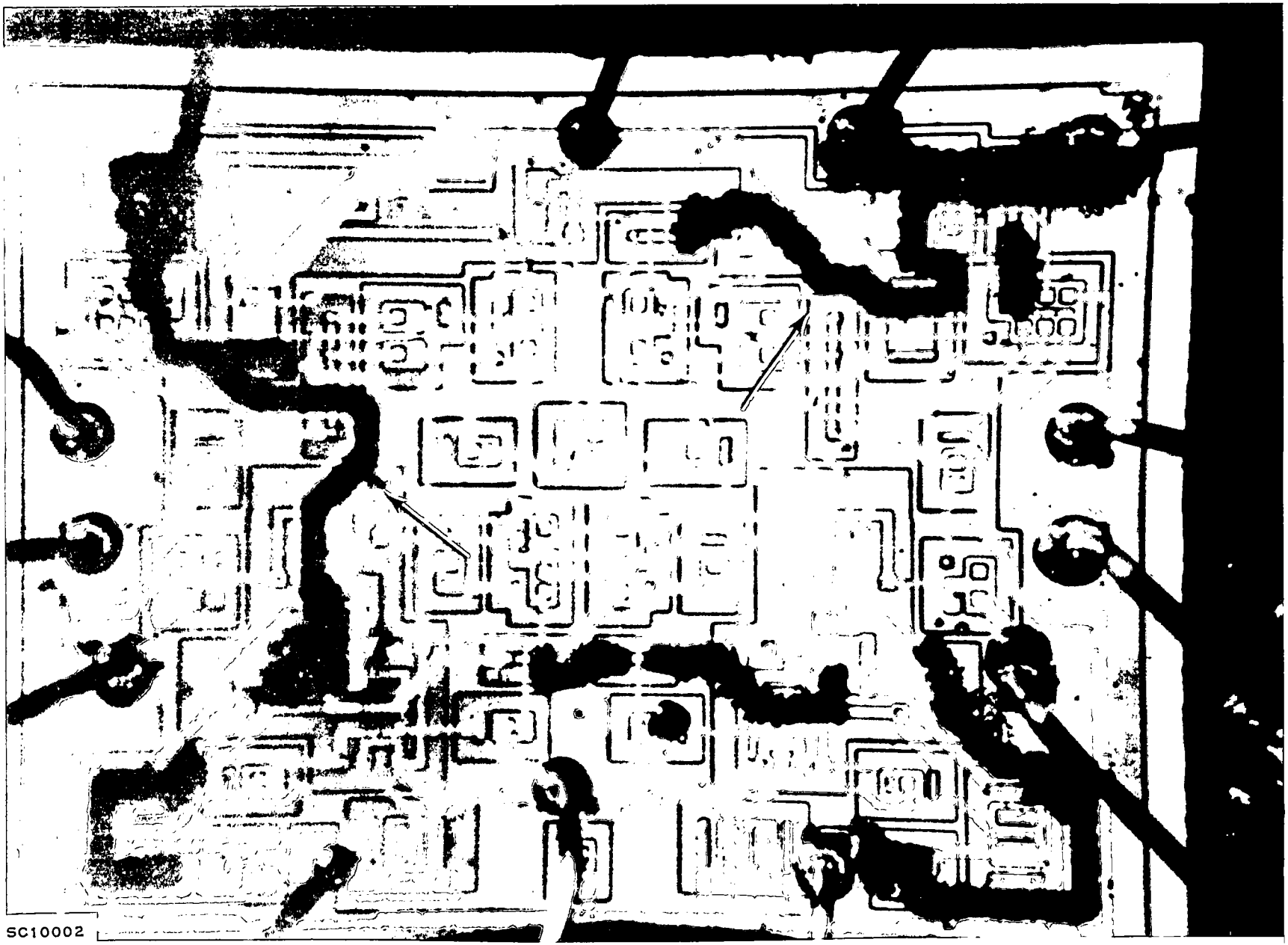


Figure 3-65. Opens due to Chemical Dècomposition

(5). Peeling of Evaporated Leads

(a). Peeling from Contact Window. In Figure 3-66, an example of an evaporated lead that has peeled from a contact window is shown. In this illustration, the metallization failed to adhere to the bare silicon contact window. This defect would be detected in preliminary threshold or pin-to-pin measurements. At times this type of defect has intermittent characteristics and can be temporarily "healed" by application of voltage or by probing, thus complicating the analysis of the device. The cause of this lack of adherence could be incomplete removal of oxide from the window, moisture in the package, residue on the die, or improper barrier metallization beneath the gold.

(b). Peeling from the Oxide. A severe case of evaporated leads separating from the oxide (die) is illustrated in the photograph shown in Figure 3-67. The open circuits and short circuits would be detected in threshold and pin-to-pin tests, although the results obtained in those tests would be thoroughly confusing prior to visual examination. This separation of the leads from the die was caused by moisture which had entered the package through a hermetic-seal leak. This failure mode is, of course, time-dependent.

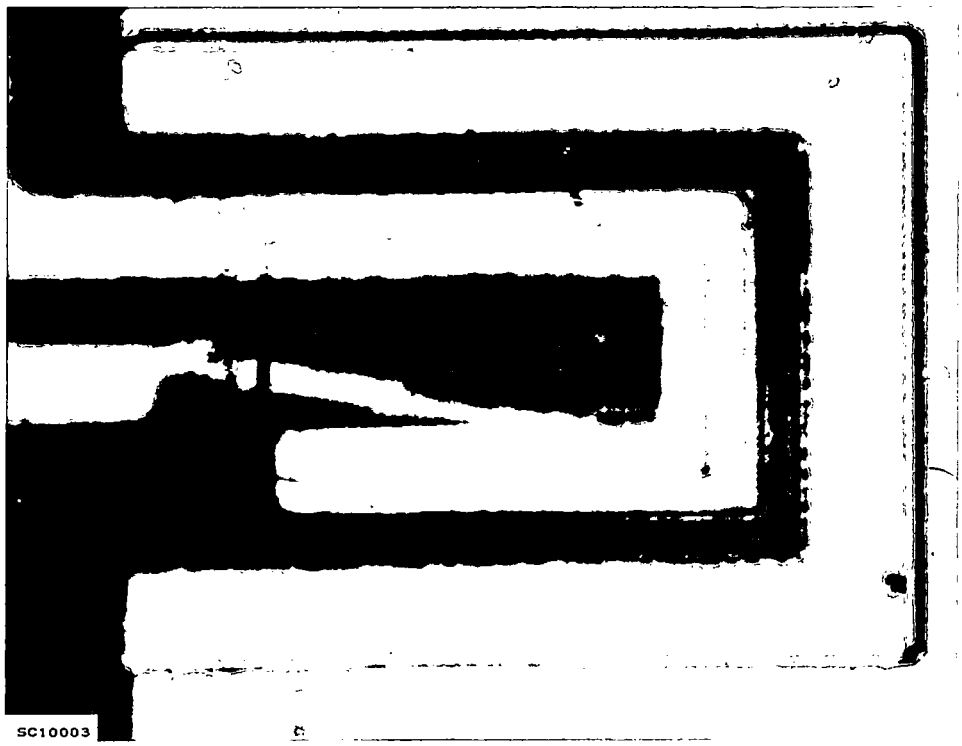


Figure 3-66. Lead Peeling from Window

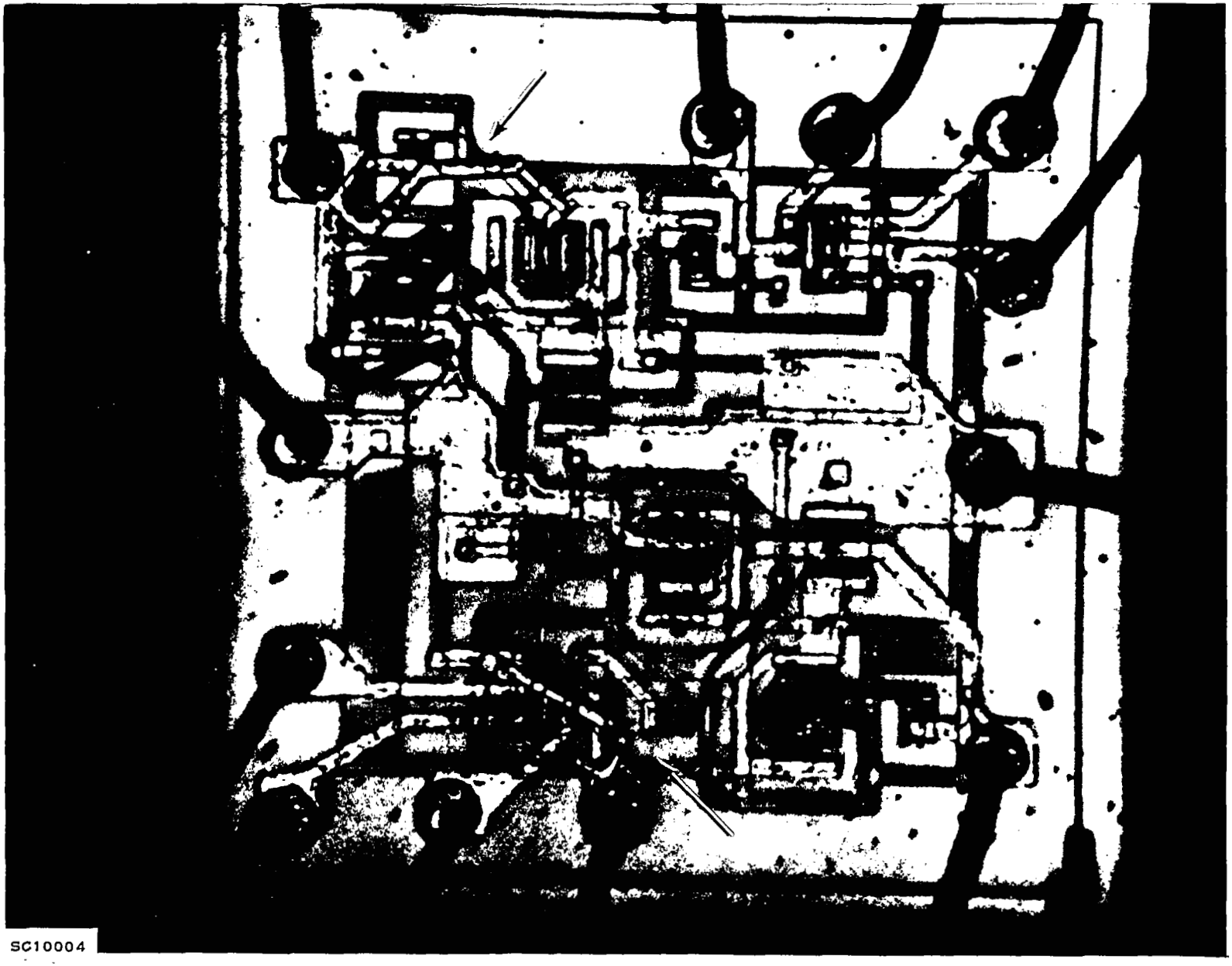


Figure 3-67. Leads Peeling from Oxide

d. Die Problems

(1). Cracked Die. The two fractures of the cracked die shown in Figure 3-68 would give varying indications on the threshold and pin-to-pin measurements. Various fractures show as open circuits, short circuits, high or low resistances, or low breakdowns. At times, threshold or pin-to-pin measurements do not indicate the fracture, making it necessary to use parameter analysis. Fractures or cracks in the die may be caused by several different factors such as improper scribing and breaking, excessive bonding pressure, large voids in the pyroceramic under the die, excessive localized heating of the die, or mechanical overstress of the package.

(2). Broken Die from Mechanical Overstress. A die which has been broken as badly as the one shown in this photograph (Figure 3-69) indicates that the package has been overstressed mechanically beyond the design limits of the device. Visual indicators are the separation of the die from the pyroceramic or the pyroceramic from the package, the badly shattered pyroceramic, and the badly shattered die. This defect would be detected in isolation tests, threshold tests, or pin-to-pin measurements and X-ray. External visual inspection and hermeticity tests may also indicate the presence of a broken die prior to opening the device.

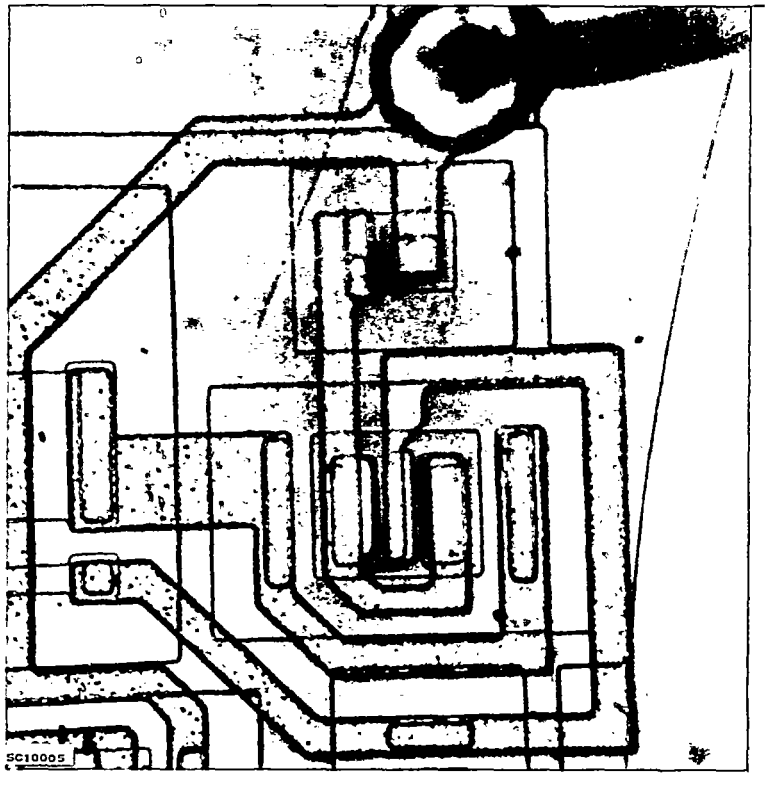


Figure 3-68. Cracked Die

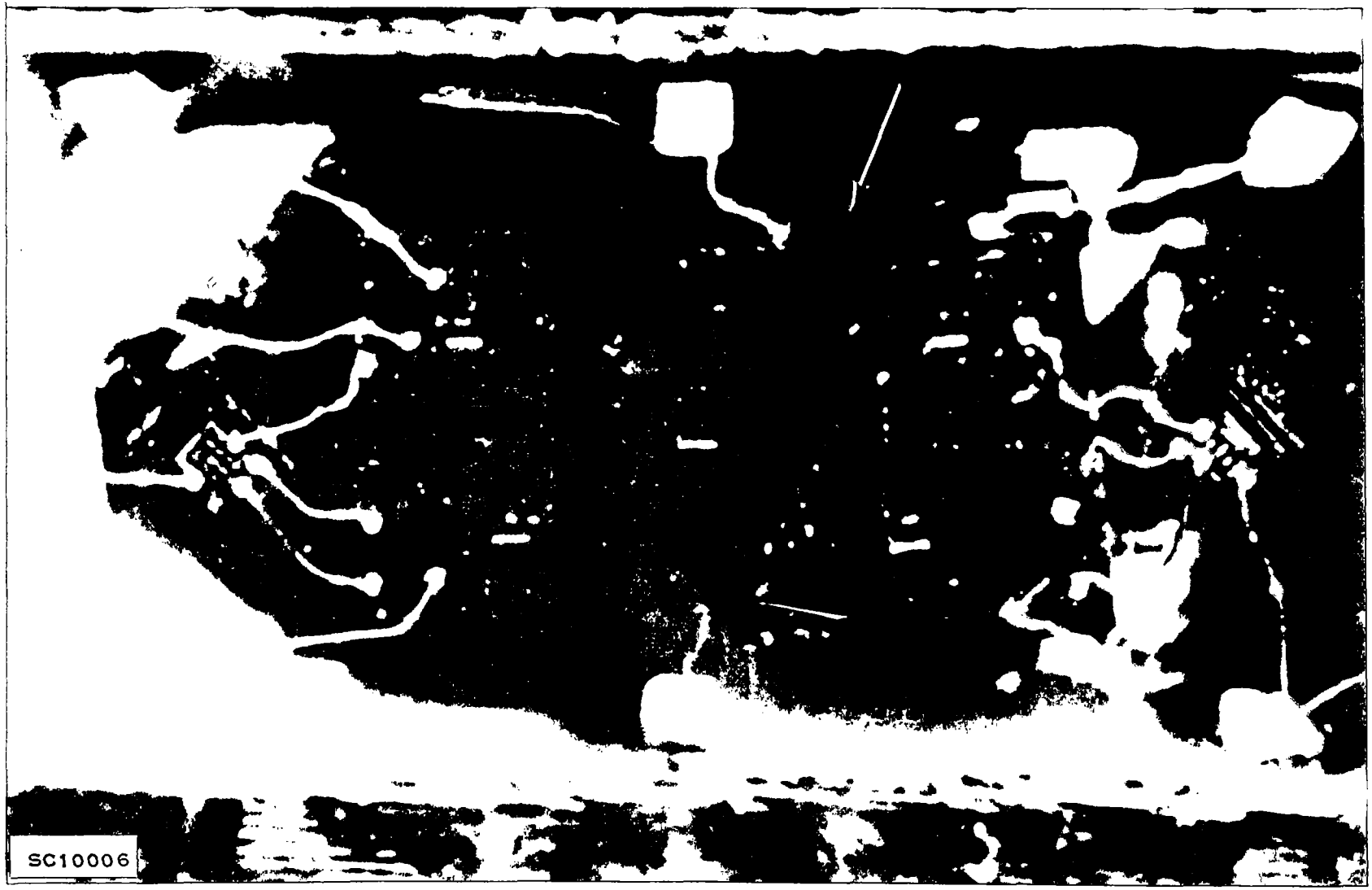


Figure 3-69. Broken Die

(3). Chipped Die

(a). Short Circuit. The chip on the edge of the die shown in Figure 3-70, resulted in a short circuit from the ball bond to bare silicon. Chips on the edge of the die may be caused by improper scribing and breaking or improper handling of the die. The chips are usually indicated by short circuits, leakages, or low breakdown-voltages on the curve-tracer threshold or pin-to-pin measurements.

(b). Open Circuit. With reference to Figure 3-71, the chipped silicon in this photograph caused an intermittent open circuit. This defect would be detected in monitored vibration tests and possibly threshold tests. The cause for this chip in the die is excessive pressure used in the ball bonding operation.

e. Connecting Wires

(1). Broken Connecting Wire. The broken connecting wire shown in this photograph, Figure 3-72, would be detected in preliminary threshold tests as an open circuit. The position of the wire indicates that there was considerable tension on the wire and that it had been bent sharply at the ball bond. The wire also shows "necking" at the break, which further indicates excessive tension.

(2). Improper Lead-Wire Routing. Improper lead wire routing is illustrated by Figure 3-73. The shorted connecting wires in this photograph would be detected in curve-tracer threshold testing or pin-to-pin analysis. This defect is the result of a workmanship error in that the wire is excessively long and improperly routed. Failure is usually induced by heat, vibration or acceleration.

f. External Terminals

(1). External Terminals Shorted to Each Other. For an example of external terminals shorted to each other, see Figure 3-74. This example shows the external terminals shorted where the pins are wrapped around the mechanical carrier for the package. This type of defect, normally detected during curve-tracer threshold testing or pin-to-pin analysis, is usually caused by rough handling during testing operations.

(2). External Terminal Shorted to the Die. This photograph, Figure 3-75, illustrates the problem of an external terminal (No. 5) that is in contact with the edge of the die, thus resulting in a short to substrate from that terminal. This defect would be detected in the preliminary curve-tracer threshold test or in pin-to-pin tests. The defect is caused by improper positioning of the die in the case. The die is mounted too high and is not centered in the case.

Figure 3-70. Chipped Die (Short Circuit)

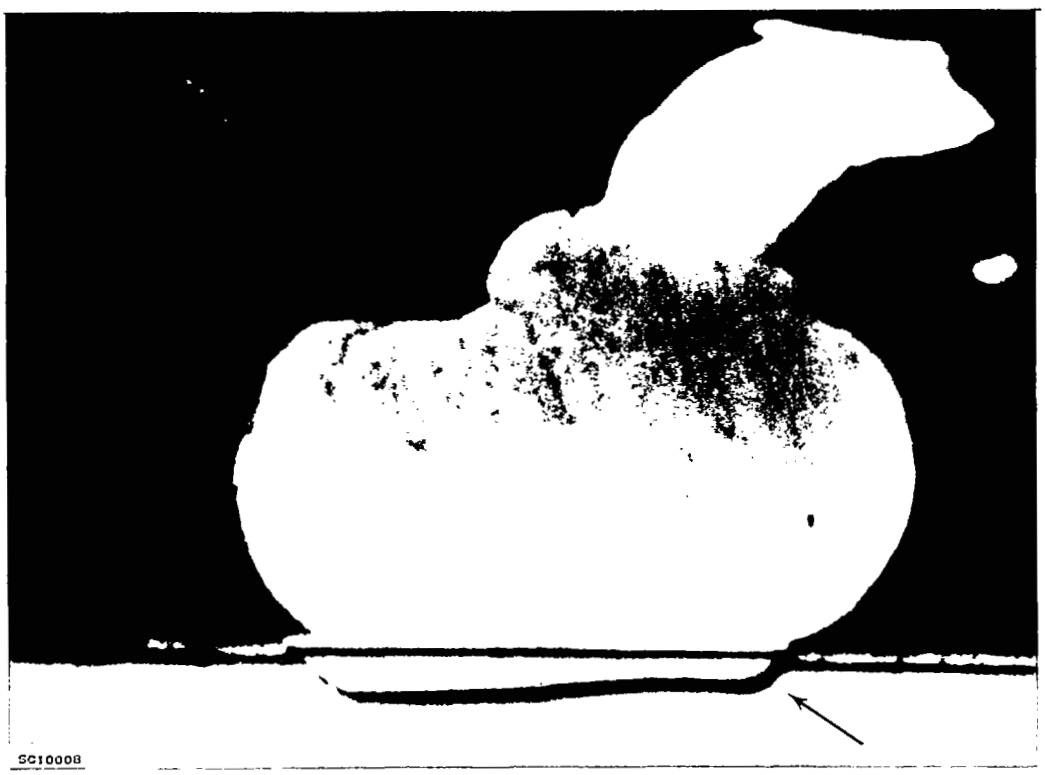


Figure 3-71. Chipped Die (Intermittent Open Circuit)

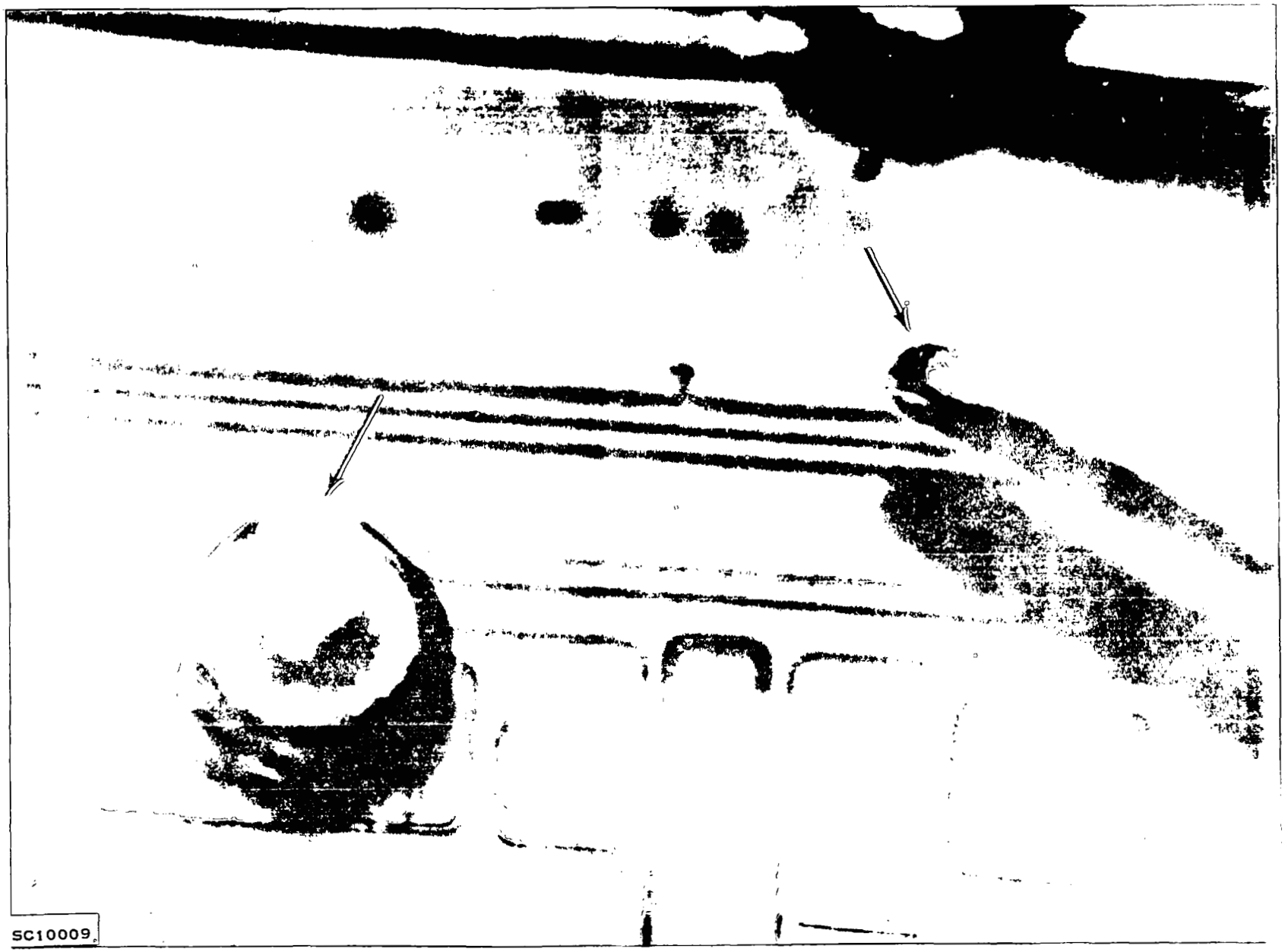


Figure 3-72. Open Circuit Due to Broken Connecting Wire

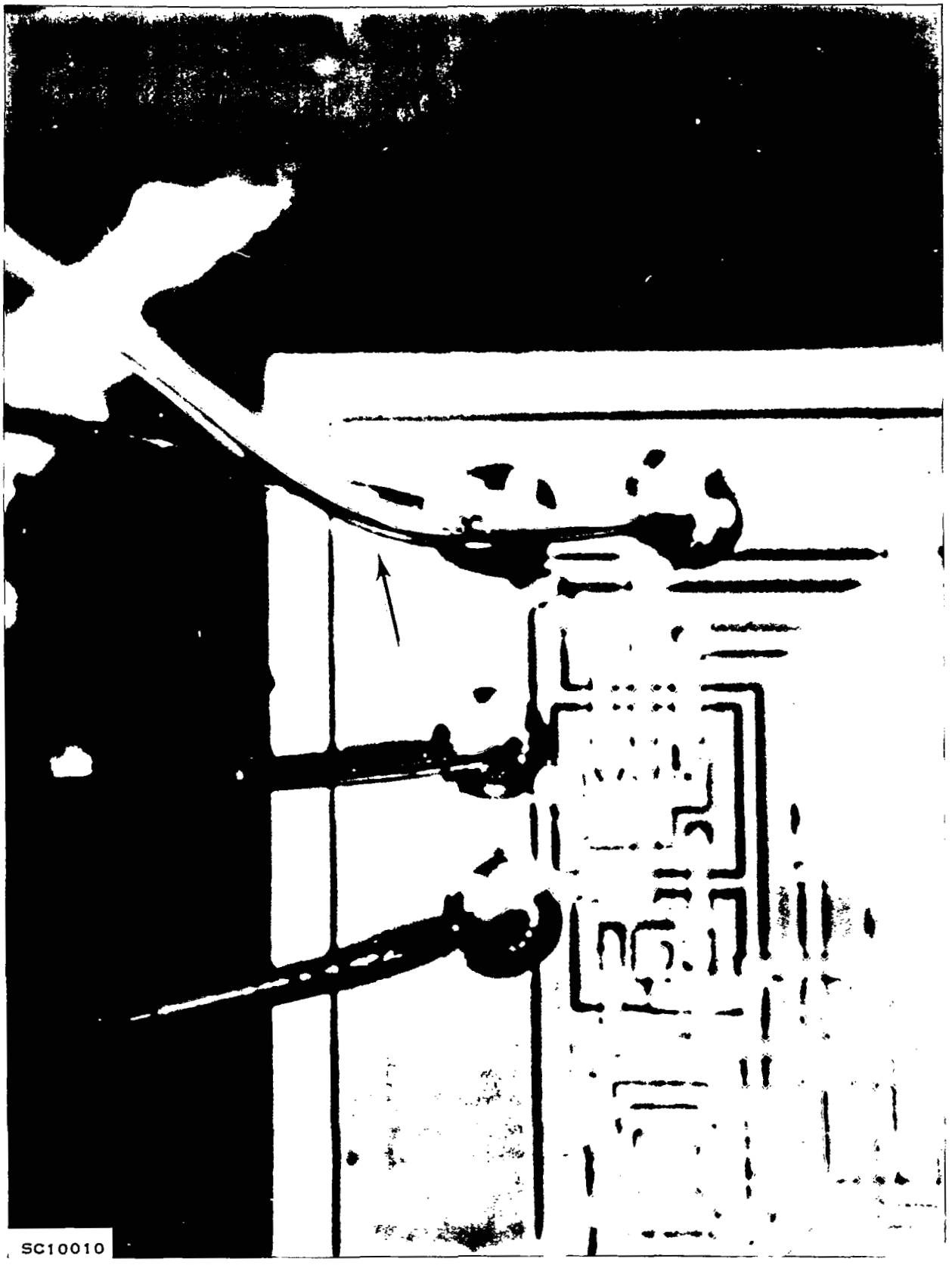


Figure 3-73. Shorted Wires Due to Improper Routing

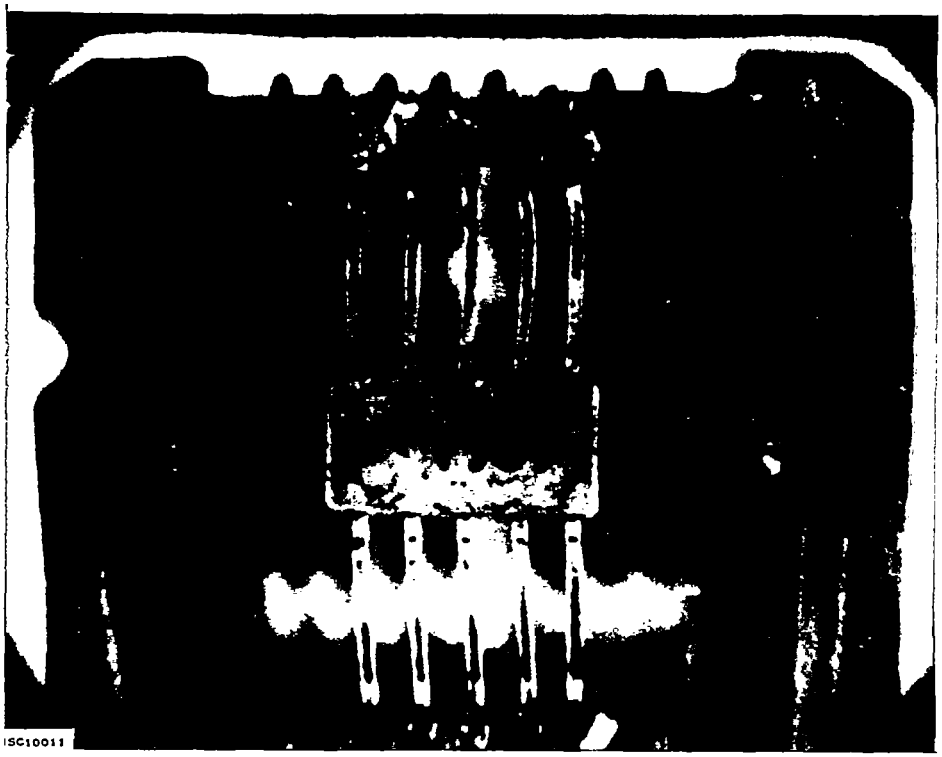


Figure 3-74. Mech-Pack Leads Shorted

(3). External Terminals Shorted to the Case. The external terminals on the device shown in Figure 3-76 were not centered in the glass eyelet, which resulted in short circuits to the case. This would be detected by preliminary isolation tests. This failure mode could be intermittent, depending on temperature and vibration.

g. Electrical Overstress

(1). Evaporated Lead Melted Open. This example of a melted-open evaporated lead, Figure 3-77, is typical of what is found when a device has been electrically overstressed. The melting usually, though not always, occurs at a contact window or an oxide step. This open circuit (a short circuit sometimes results) would be detected in threshold or pin-to-pin measurements. If the component where the melting has occurred has not been damaged, bridging-across the open circuit by means of probes will help determine if the electrical overstress was caused by the device or by external means. If bridging the component into the circuit is not possible, each component in that portion of the circuit must be checked to determine if the cause was internal or external.

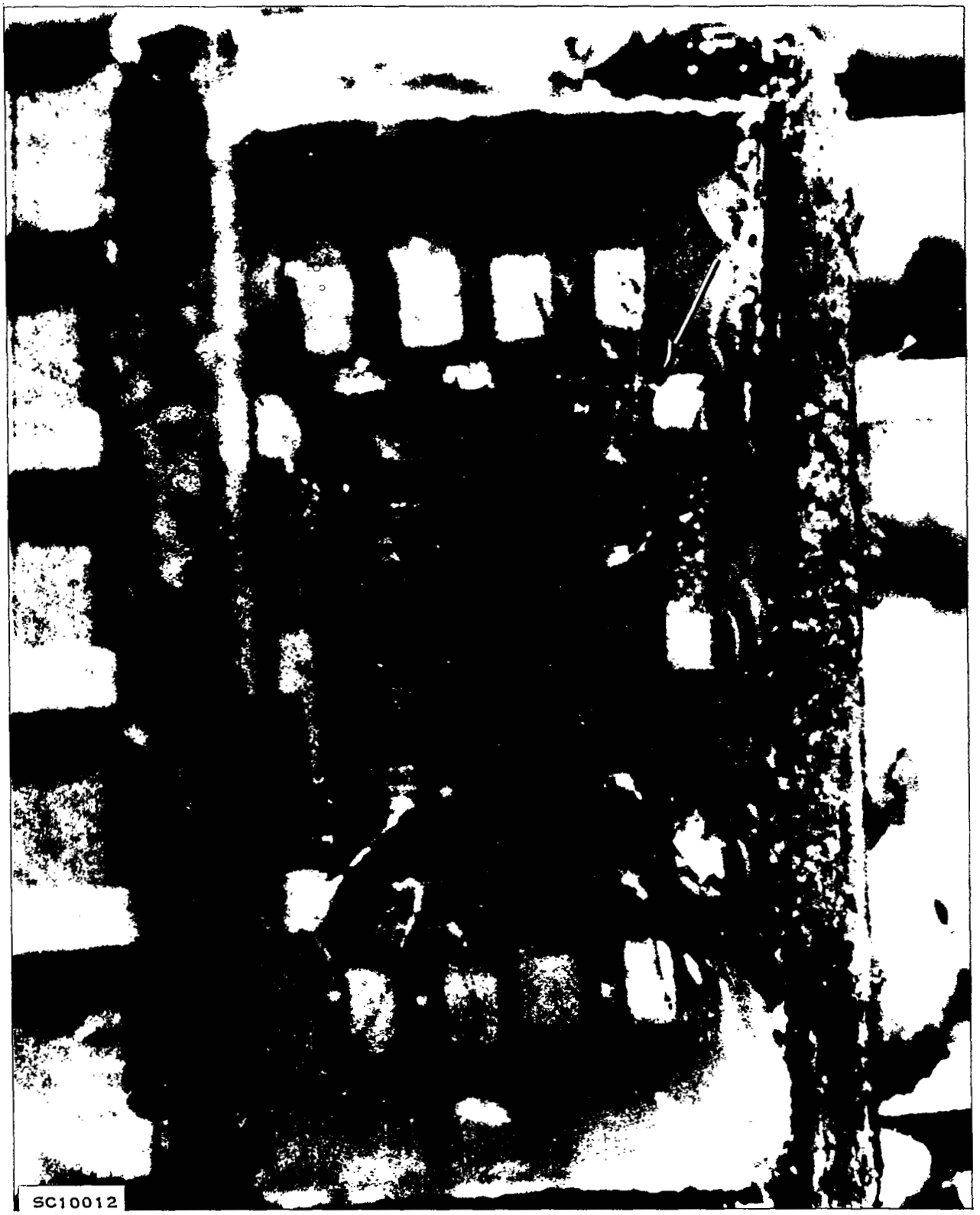


Figure 3-75. Silicon Die Shorted to External Terminal

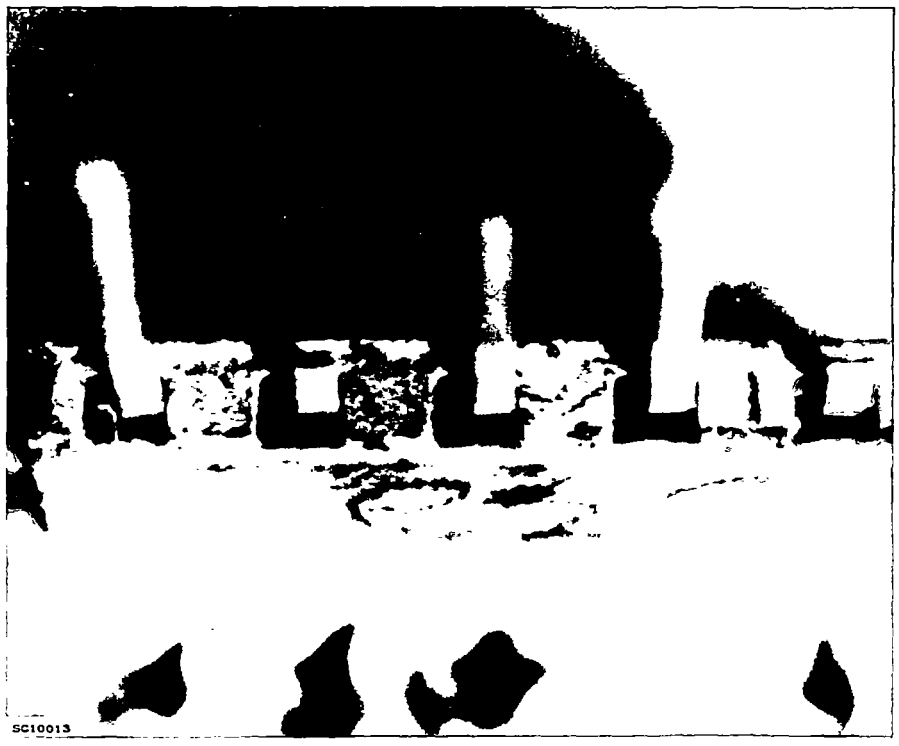


Figure 3-76. External Terminals Shorted to Case

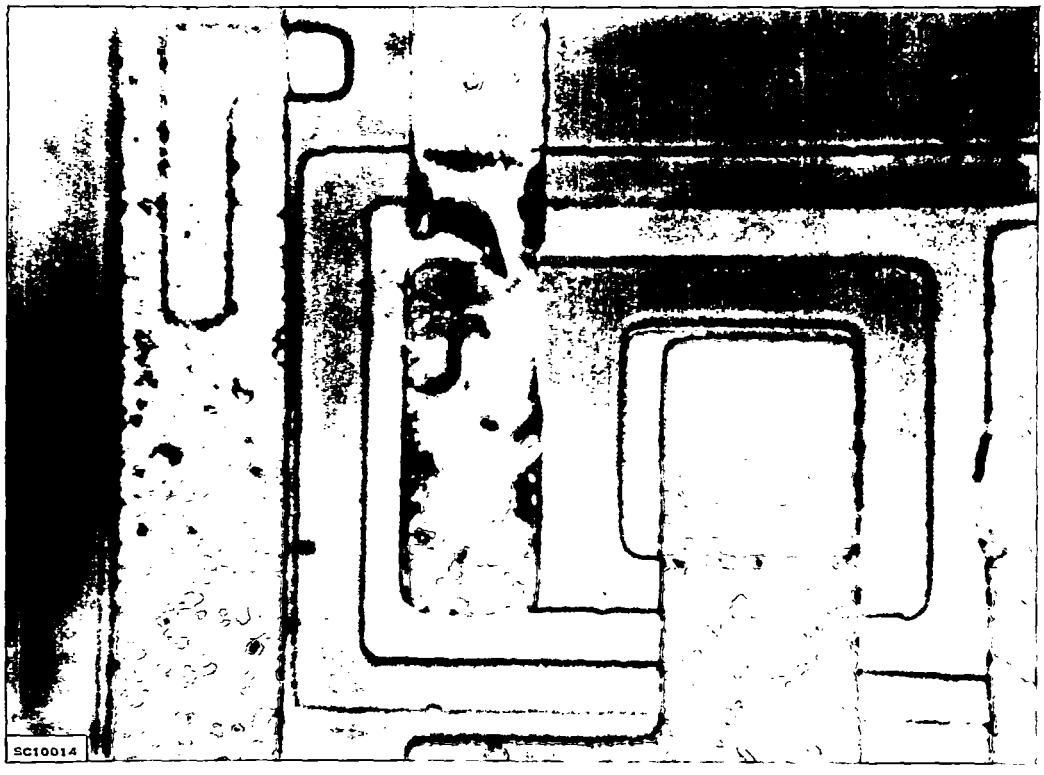


Figure 3-77. Electrical Overstress

(2). Flash-Across Short. This photograph, Figure 3-78 is typical of of what is observed when a flash-across short has occurred. The short circuit would be detected in curve-tracer threshold tests or pin-to-pin analysis. A flash-across short such as this is usually caused by reverse-bias voltage transients across junctions and is considered to have been caused by some means external to the device.

The flash-across short is one of the most frequently occurring failure modes resulting from electrical overstress. The visual symptom of this failure mode is a thin strip of metallic-appearing substance between two evaporated leads. There is always one or more PN junctions between the two evaporated leads. The most common flash-across short occurs across emitter-base junctions or across collector-emitter nodes of transistors. The flash-across short has been frequently observed between the emitters of multiple-emitter transistors or between one of the emitters and the base contact.

This failure mode may be reproduced by discharging a capacitor across reverse-biased PN junctions. The capacitance required is a function of the distance between the evaporated leads and the junction, and of the dielectric strength of the oxide to silicon interface.

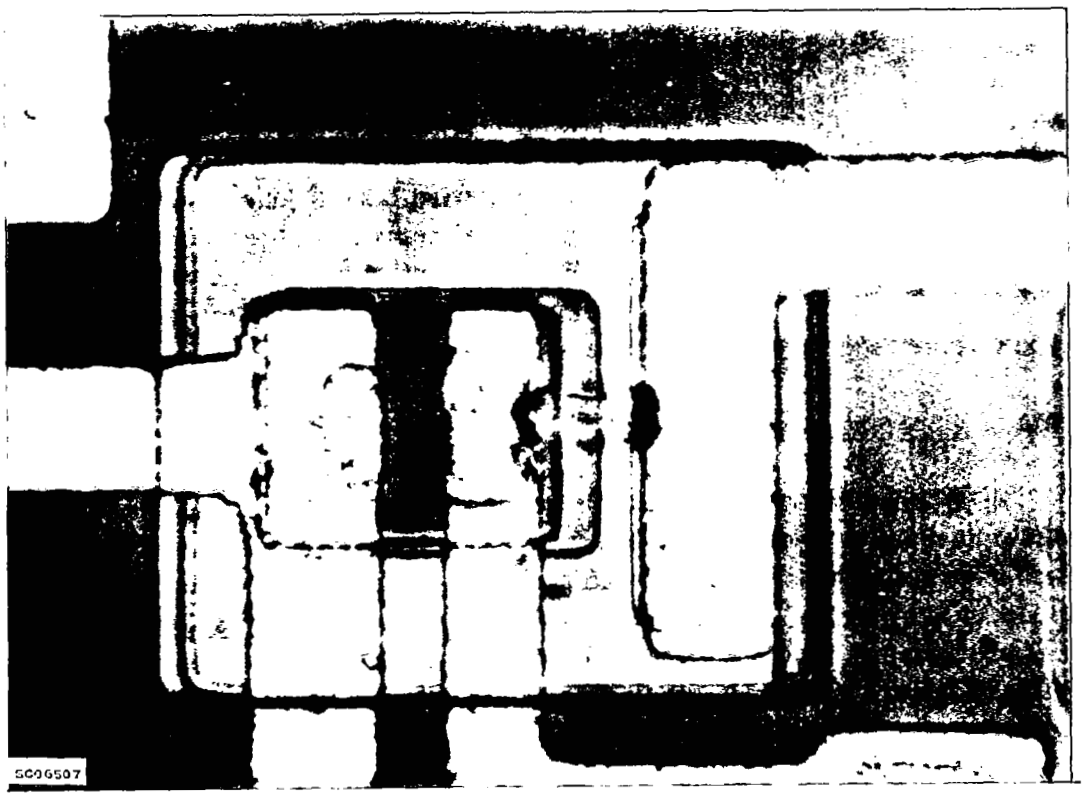


Figure 3-78. Flash-Across Due to Electrical Overstress

The flash-across properties are described by the equation

$$E = \frac{V}{d} \qquad (2)$$

where

E = the electric field that will cause an arc

V = voltage

d = the distance over which the electric field exists

The voltage, "V," of Equation (2), exists across the depletion layer of the junction. As the voltage is increased, the depletion layer spreads away from the junction and thereby increases the distance, "d." A finite time is required for "d" to increase. If "V" increases faster than "d" then "E" increases. Flash-across occurrs when the dielectric limit of the oxide-silicon interface is exceded by "E." After flash-across begins, the finite resistance of the silicon allows the arc to extend to the nearest metallization.

Microsections of flash-across shorts have indicated that the metal from the contacts arcs across, causing permanent damage to the junction. The metal movement always occurs beneath the silicon oxide at the silicon-to-oxide interface. It is suspected that arcing occurs beneath the oxide rather than above it because the dielectric is weaker at that interface. Flash-across shorts usually occur because of fast voltage-transients across reverse-biased junctions.

(3). Junction Degradation From Electrical Overstress. Electric overstress can be manifested by localized melting of the material around a PN junction, a degradation of diode action, or by flash-across shorts. Localized melting is usually associated with excessive current through forward biased junctions. Degradation of diode action can be examined by forward biased current-voltage characteristic of a PN junction. Electric overstress such as high current in the avalanche region causes higher currents at lower voltages. Decreased current gain is often symptomatic of this type of electrical overstress.

3. Correlation of Observed Problem and Original Problem Report

When a defective component or area in the microcircuit has been located, it is again necessary to refer to the original problem report. It must be determined if this defective component or area could have caused the device to fail in the manner described in the original report. The observed discrepancy may not be related to the original problem but may have resulted from electrical tests, opening the package, or the primary failure mode. If the findings correlate with the original problem report, it may be assumed that the analysis was correct and the failure mode has been determined. Often it is desirable or necessary to simulate the failure mode on a known good device to determine if the failure mode could cause the failure indicators originally described.

C. ELECTRICAL EVALUATION

1. General

Electrical evaluation after device opening should normally begin with a retest of failed parameters to determine if the condition has remained stable. Provided that stability exists, any visually observed defects should be evaluated to determine their effect on failed parameters. The type of defects normally found visually are discussed in the previous section. In this section are discussed methods of determining what effect, if any, these visual defects have on the failed conditions. In the absence of any worthwhile visual results, detailed electrical testing is required. This electrical testing requires the capability of functional probing, selective and complete lead removal, temperature cycling, and measurement of voltage-current characteristics of capacitors, resistors, diodes and transistors.

2. Special Required Equipment

a. Functional Probing Equipment

The functional probing equipment is necessary for measuring voltages and currents of the metallized leads located on the surface of the bar. A typical probe set is shown in Figure 3-79. This probe set contains two probes that are adjustable in the X, Y and Z planes by means of micromanipulators. The probes are made of approximately 5-mil diam tungsten wire which is sharpened to approximately a 1/4 mil radius of curvature by means of electrochemical etching in a mixture of detergent and sodium hydroxide, as shown in Figure 3-80(a). Proper sharpening is obtained when the probe tip is raised and lowered near the surface of the liquid to form a meniscus, as in Figure 3-80(b). The detergent reduces surface tension to the desired amount.

The probes of the probe set are connected to banana jacks, which allows connection to any type of testing equipment desirable. The probes are located in such a manner that they can make contact with the microcircuit while power is being applied to the circuit. The microcircuit normally is mounted on a fingerboard to which power is applied. Probe sets may consist of more than two probes; however, two probes per set has been found to be quite satisfactory for normal failure analysis.

b. Selective and Complete Lead Removal Equipment

Selective lead removal is accomplished by a battery-capacitor circuit, shown in Figure 3-81. Initially the spring loaded switch is in position A, with the capacitor being charged by the battery. The objective is to melt a small portion of the metallization to cause a small opening across the width of the lead. This is accomplished by throwing the switch to position B, thereby discharging the capacitor through the probes and the portion of lead between the probes. Sufficient heat is produced by

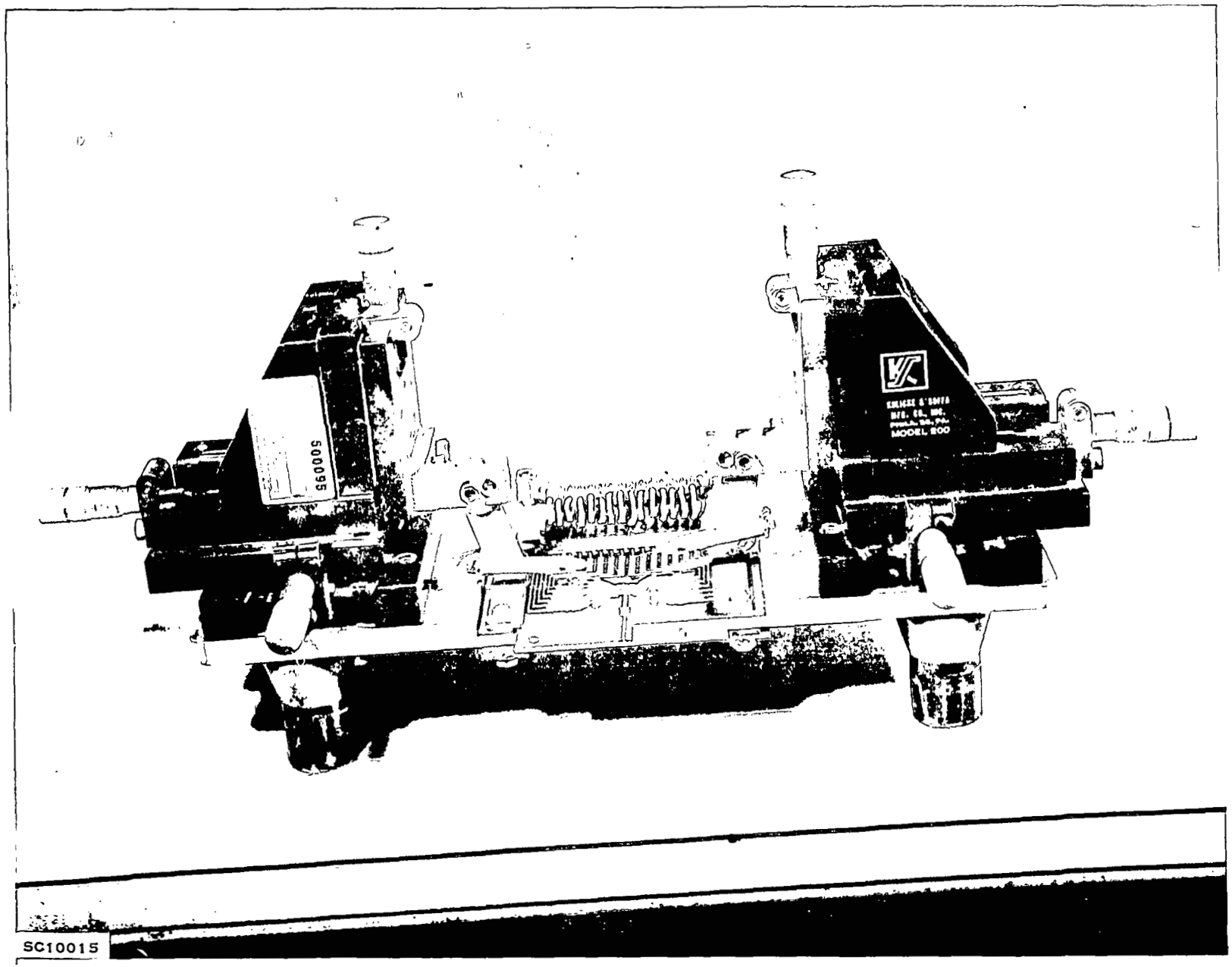
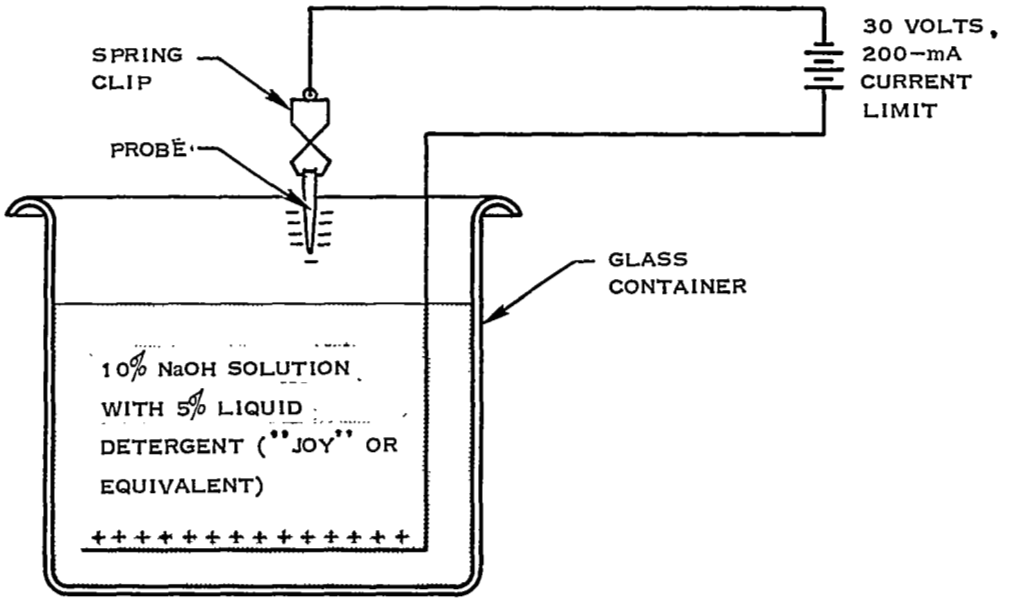
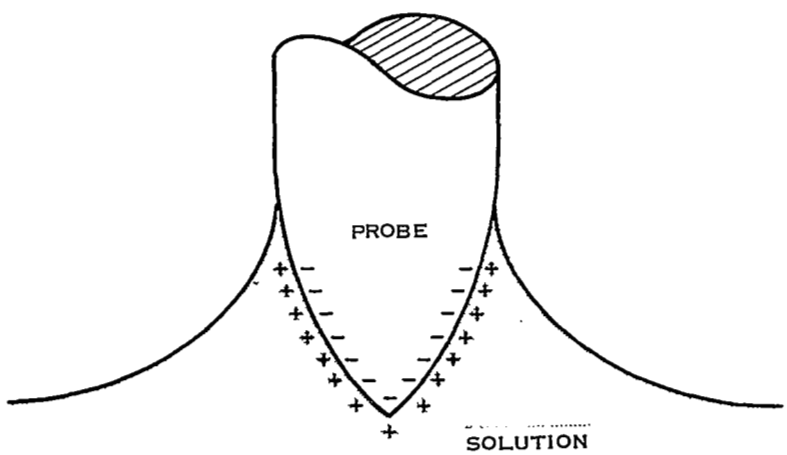


Figure 3-79. Probe Set



(A) ELECTRICAL CIRCUIT FOR PROBE SHARPENING



(B) MENISCUS LOCATION FOR PROPER SHARPENING

SC08202

Figure 3-80. Tungsten Probe Sharpening Technique

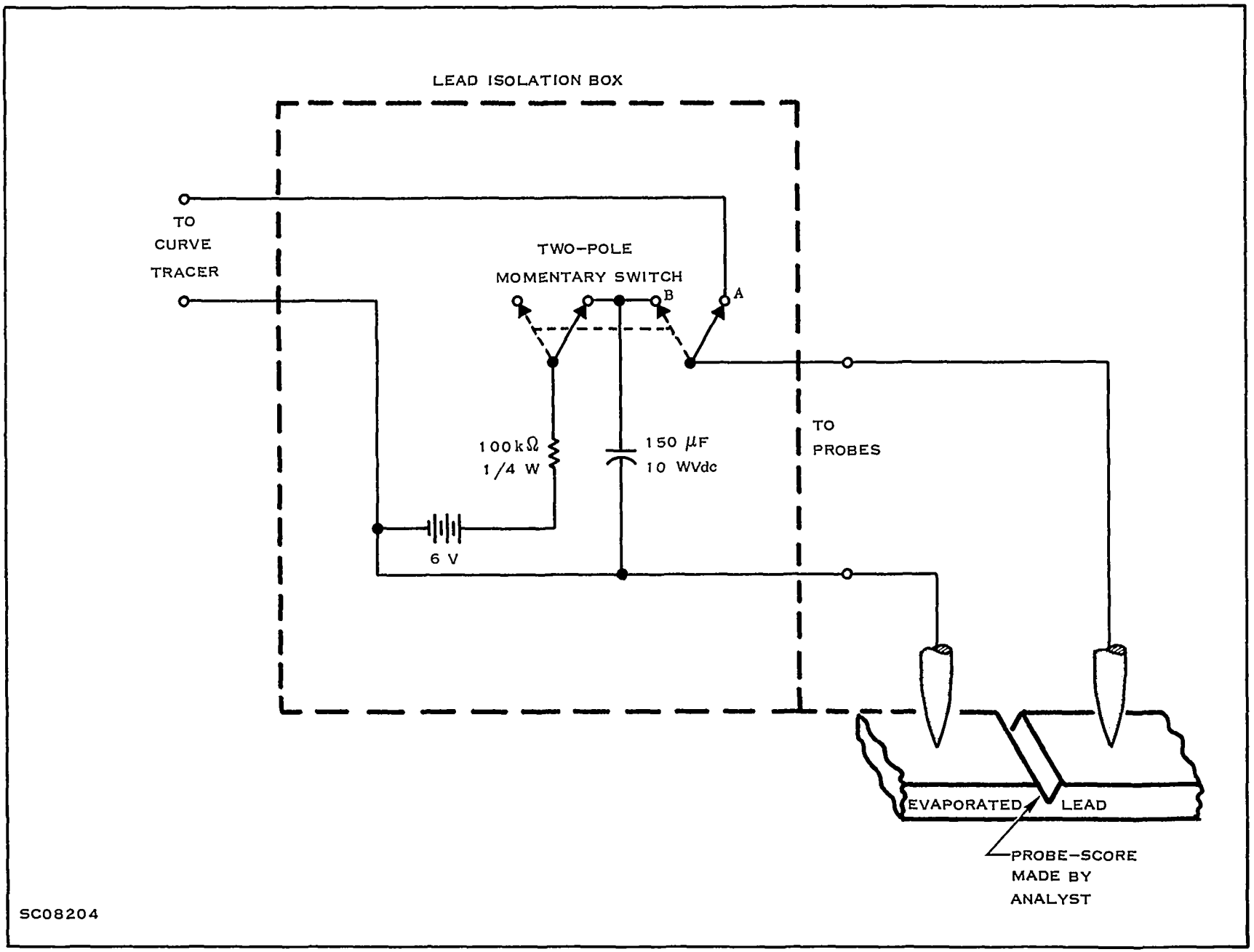


Figure 3-81. Lead-Opening Circuit

the passage of current through the lead to cause melting. Often it is advantageous to scratch the lead where the open is desired, to accelerate the melting. As soon as the spring-loaded switch is released, the battery is reconnected to the capacitor and recharging occurs. The device is immediately capable of a second application of current in case the first discharge was not adequate. The size of the capacitor must not be too large, since excessive heat produces oxide damage and leakage. In the case of a multilayer metallization, a curve tracer may be used to assist the capacitive discharge. This may be accomplished by connecting the curve tracer, adjusted for 5 V across the probes, immediately after the capacitor is discharged. The schematic shown in Figure 3-81 is one method of incorporating the curve tracer with the capacitor-discharge.

c. Patching Lead Openings

The previous paragraph discussed a method of opening a lead by melting. It is desirable in some cases to reconnect the leads for additional electrical evaluation tests. One method is to jumper together two probes, placing one on each side of the open place. This is satisfactory for a single open but is not feasible where a number of opens have been made. A solution to the problem is provided by use of a conductive epoxy paste ("Eccobond" or equivalent). The epoxy paste is prepared by mixing the two supplied materials according to the manufacturer's instructions. The paste is applied to the open in sufficient quantity to fill the gap. One method of application is by transporting small quantities with the tip of a probe.

d. Temperature Cycling Equipment

Device operation at temperature extremes may be required to evaluate intermittent or temperature sensitive conditions. High temperature may be obtained with a hot air blower or heat gun. More precise temperatures may be obtained with a controlled soldering iron by combining it with a thermocouple measurement circuit to provide temperature indication. The hot tip is placed in contact with the unit under test. Where this is not practical, any oven may be utilized. Low temperatures in the range of −50°C to −70°C may be obtained with dry ice in direct contact with the unit under test.

e. Removal of Metallization

It is occasionally necessary to remove metallization from the surface of a bar to observe defects which exist beneath the metallization. The materials to be used for this task depend upon the type of metallization existing on the bar. In the case of aluminum metallization, hydrochloric acid will remove the aluminum and leave a clean oxide surface. For a multilayer metallization such as gold molybdenum, aqua regia is required. Aqua regia is made by mixing three parts of hydrochloric acid to one part of nitric acid. A water wash should be used after any of the metallization removal techniques to clear away the residual acid.

CAUTION

Acid fumes are harmful when inhaled. Some method of exhausting the fumes, such as a fume hood, should be used when working with acids.

Microsectioning is frequently necessary in order to determine the condition that caused failure. This is fully described in Section V of this volume. Occasionally, determination of the chemical content of certain foreign materials is required. The chemical analysis techniques used for this purpose are described in succeeding paragraphs.

3. Digital Circuits

a. General

The electrical evaluation which follows after the device has been opened and visually examined may be divided into two categories: verification of observed defects, and determination of nonobserved defects.

b. Verification of Visually Observed Defects

When seeking to verify visually observed defects, the analyst is concerned primarily with determining that an observed visual defect did or did not contribute to device failure. For example, a visual indication that a "no output symptom" was caused by a scored evaporated lead pattern may be verified by probing the lead continuity at the location of the score or scratch. A suspected junction defect may be verified by probing to determine the junction characteristics. It is usually necessary to isolate the component from the remainder of the circuit in order to accomplish this. Isolation of components requires opening of the evaporated leads which interconnect the components on the die.

Verification of visual defects is an important part of the electrical evaluation of a device. All visual defects should be investigated; however, the presence of a visual defect does not necessarily mean that portion of the circuit does not function properly or that the visual defect would cause failure at a future date. The effectiveness of visual screening for reliability improvement is a much discussed topic among reliability engineers. The information that a particular defect was observed but did not contribute to failure is often as worthwhile as the defect which did cause failure.

c. Locating Defects not Visually Observable

To identify visually nonobservable defects is usually much more difficult than verification of visual defects in that the defective area or component must first be located. Parameter evaluation is often quite helpful in locating the defective

area, since the parameters are designed to insure that each portion of the circuit performs the proper function. The parameters, however, do not always provide enough information to enable the analyst to locate the defective area. When this is the case, electrical probing of the device while it is under failure conditions is useful.

d. Typical Examples of Evaluation Problems

(1). An Open Circuit. An open circuit is a typical evaluation problem. One such example is the case of the TTL gate which exhibited the failure symptom that "the output does not go 'high' when a 'low' voltage is applied at any of the four inputs." The schematic diagram for a TTL gate is shown in Figure 3-82. This voltage values illustrated in Figure 3-82 are those which should typically be expected from the device if the inputs are grounded and the output is supplying 400 μA of current. Electrical probing revealed that the voltage was actually as shown in Figure 3-83.

Examination of the voltages indicated that an open existed in the base circuitry of the "high" side of the output transistor. Further probing, as shown in Figure 3-84,, revealed an open circuit which was not observable by visual examinations. Absolute verification of the open evaporated lead was obtained by bridging across the open circuit and observing that the device performed satisfactorily. The desirability of the bridging, or patching, technique may be judged by the fact that not only was the open circuit verified, but satisfactory operation proved that this was the only cause of failure for the device.

(2). A Degraded Component. Defects such as degraded components are usually nonobservable defects, visually. The characteristics shown in Figure 3-85 would be exhibited by a RCTL gate if the device were functioning properly. A defective device might exhibit the characteristics shown in Figure 3-86.

Analysis of the circuit of Figure 3-86 indicates that the Q-output transistor is not saturated. The gain of a transistor is, by definition, the collector current divided by the base current, at a given V_{cc} potential. A circuit analysis of Figure 3-85 reveals that the gain of the output transistor must be high enough to sink the current which flows through the 5-kΩ resistor, with the base drive supplied through the 20-kΩ input resistors. The required gain is calculated in the following manner:

$$h_{FE} = \frac{I_C}{I_B} \tag{3}$$

where

h_{FE} = static value of the forward current transfer ratio (common emitter)

I_C = collector current (dc)

I_B = base current (dc)

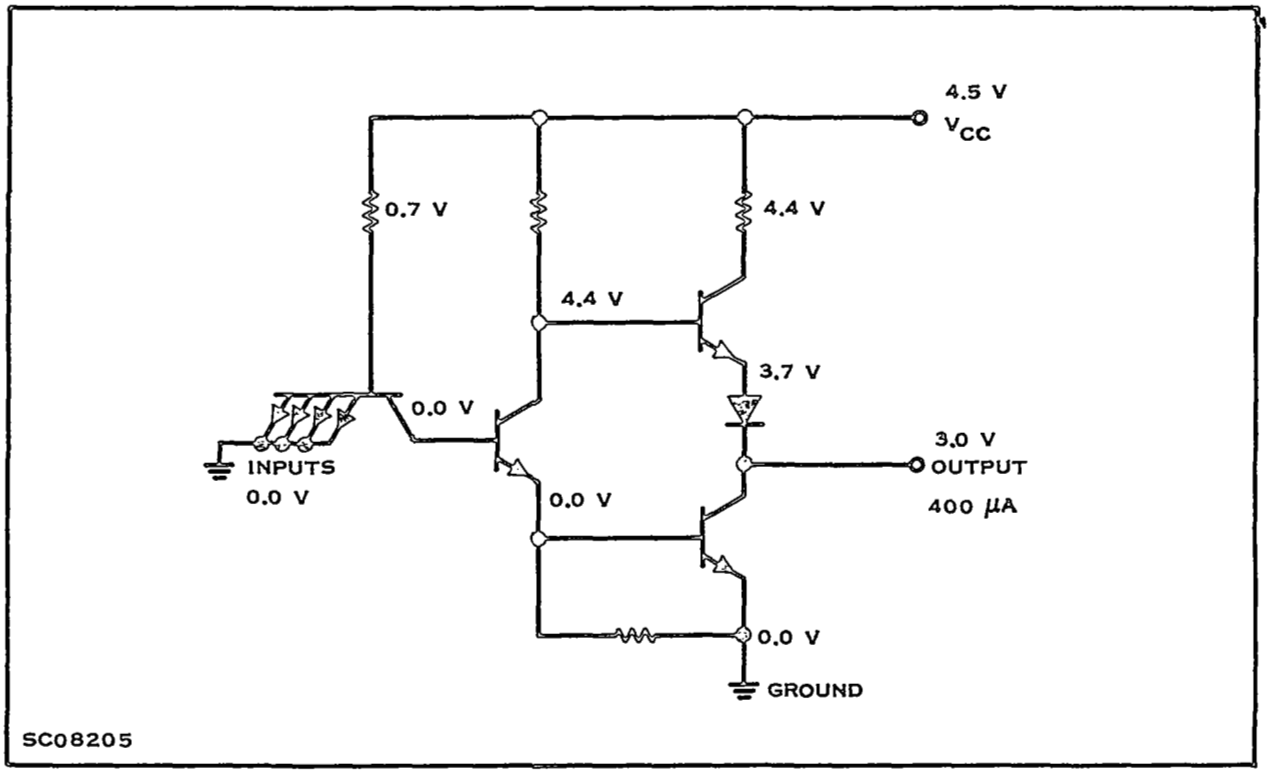


Figure 3-82. Expected Voltage Values of Good TTL Gate

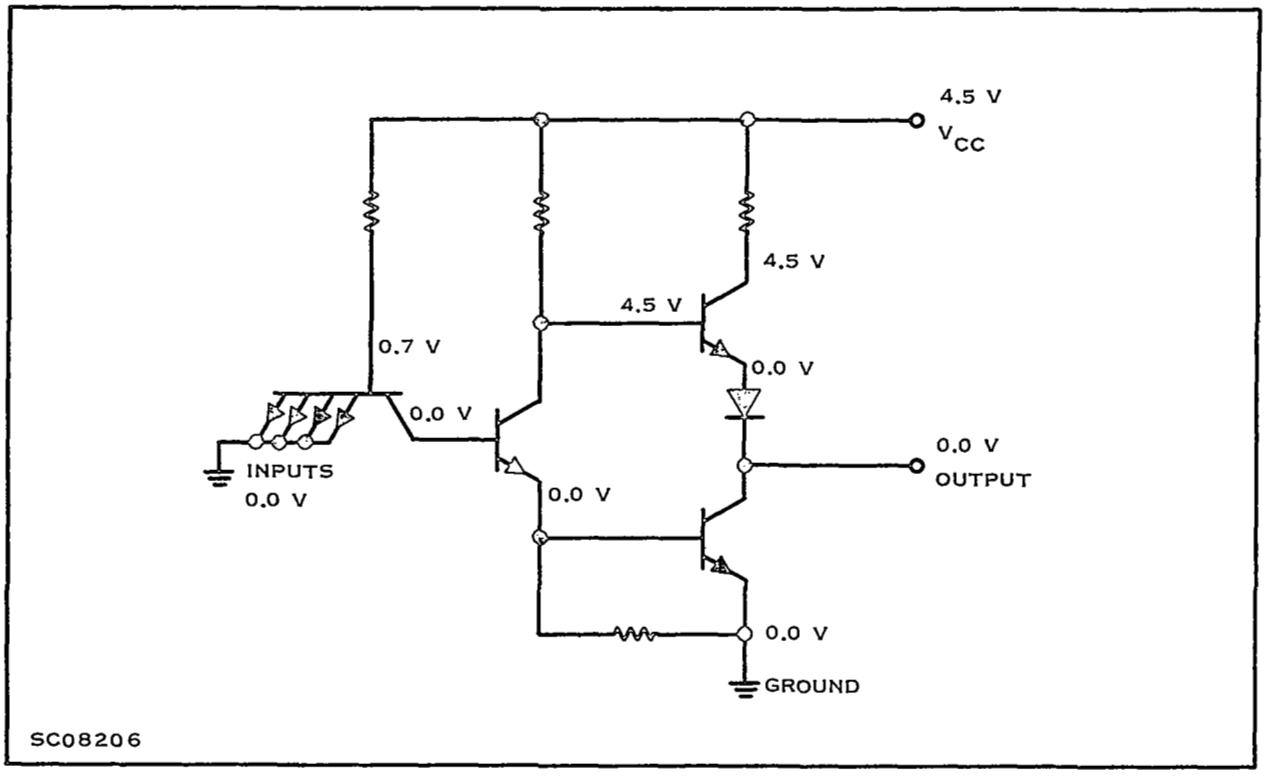


Figure 3-83. Actual Voltage Values of Defective TTL Gate

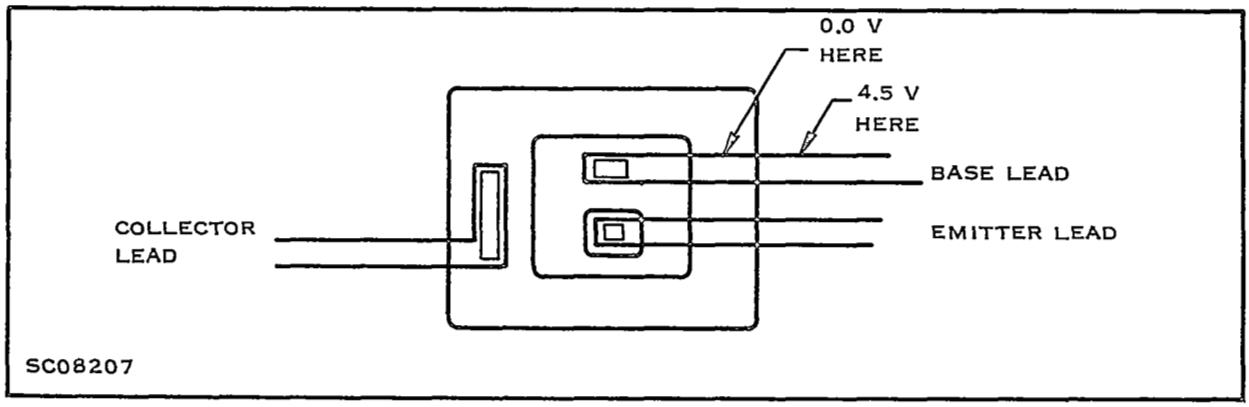


Figure 3-84. Measured Voltages of Defective TTL Gate Transistor

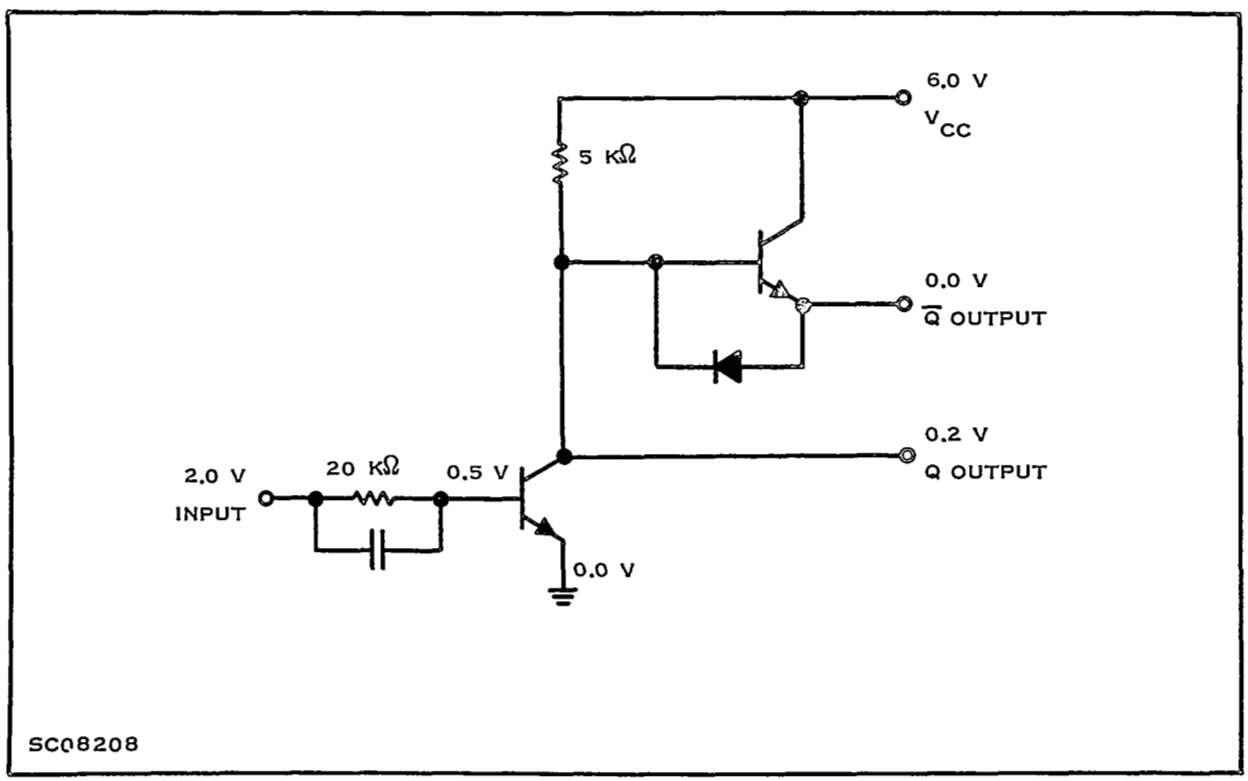


Figure 3-85. Expected Voltage Values of Good RCTL Gate

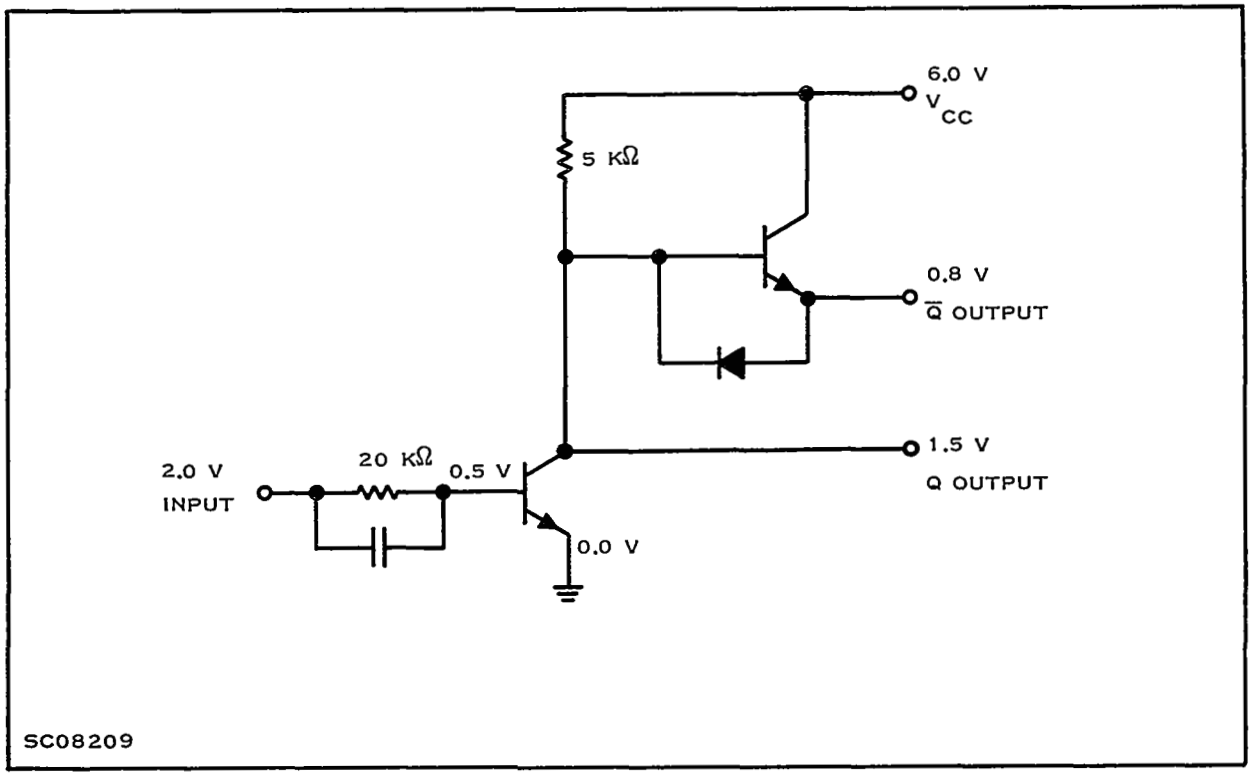


Figure 3-86. Actual Voltage Values of Defective RCTL Gate

$$\frac{I_C}{I_B} = \frac{\dfrac{V_{CC} - V_{CE}}{R_L}}{\dfrac{V_{in} - V_{BE}}{R_{in}}} \tag{4}$$

where

V_{CC} = collector supply voltage (dc)

V_{CE} = collector-to-emitter voltage (dc)

R_L = load resistor

R_{in} = base resistor

V_{in} = input voltage

V_{BE} = base-to-emitter voltage (dc)

therefore,

$$h_{FE} = \frac{\frac{6.0 - 0.2}{5k}}{\frac{2.0 - 0.5}{20k}} = 15.5$$

Thus, a gain of 15.5 is required for the Q transistor to saturate.

Isolation of the Q-output transistor will provide the information required concerning the transistor. Lead isolation is performed by opening the evaporated lead pattern, as shown in Figure 3-87. A gain of less than 15.5 would verify the cause of the unsaturated transistor. With the defective component located and isolated, failure analysis may then be continued to determine the cause for low transistor gain.

(3). A Shunted Circuit. Examples of an open circuit and a degraded component have demonstrated the necessity of a good electrical evaluation after opening the device. A third example, a shunted circuit, is typified in the case of a DTL gate with a slow fall-time on the output. Typical voltage nodes with the gate in the "on" condition are shown in Figure 3-88. The actual existent condition shown in Figure 3-89 indicated that the anode to the inputs was being "clamped" by a shunt path, which caused the output to fall slowly.

The lead pattern common to the anodes of the input diodes was isolated, as shown in Figure 3-90. Upon probing the isolated lead segment, it was revealed that a shunt path of 3kΩ existed between the lead and substrate (ground). This shunt path was starving the base drive of the output transistor, resulting in a condition of minimum saturation. Minimum saturation of the output caused slow fall time at the output. Further lead isolation, and subsequent removal of all leads, revealed an oxide defect beneath the evaporated lead at a point where that lead crossed over the substrate material.

Electrical evaluation after the device has been opened should be carefully performed and correlated to the failure symptoms of the device. A careful evaluation will invariably locate and isolate the defective region, and will ultimately lead to successful failure analysis of the device.

4. Linear Circuits

a. General

This part of Section IV presents a discussion of the electrical evaluation of linear circuits. The term "linear" is used here to mean the straight-line relationship of a microcircuit's input to its output over the useful range of the device.

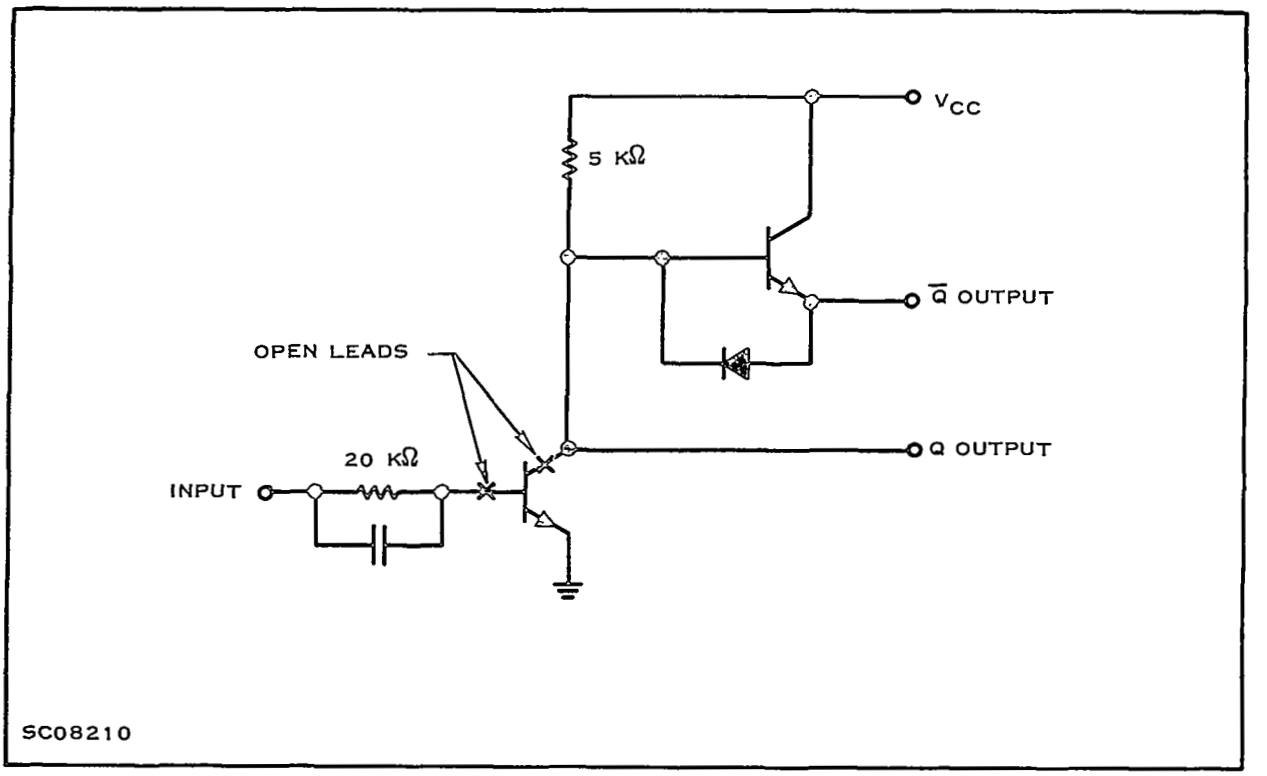


Figure 3-87. Lead Openings Required to Isolate Q-Output Transistor

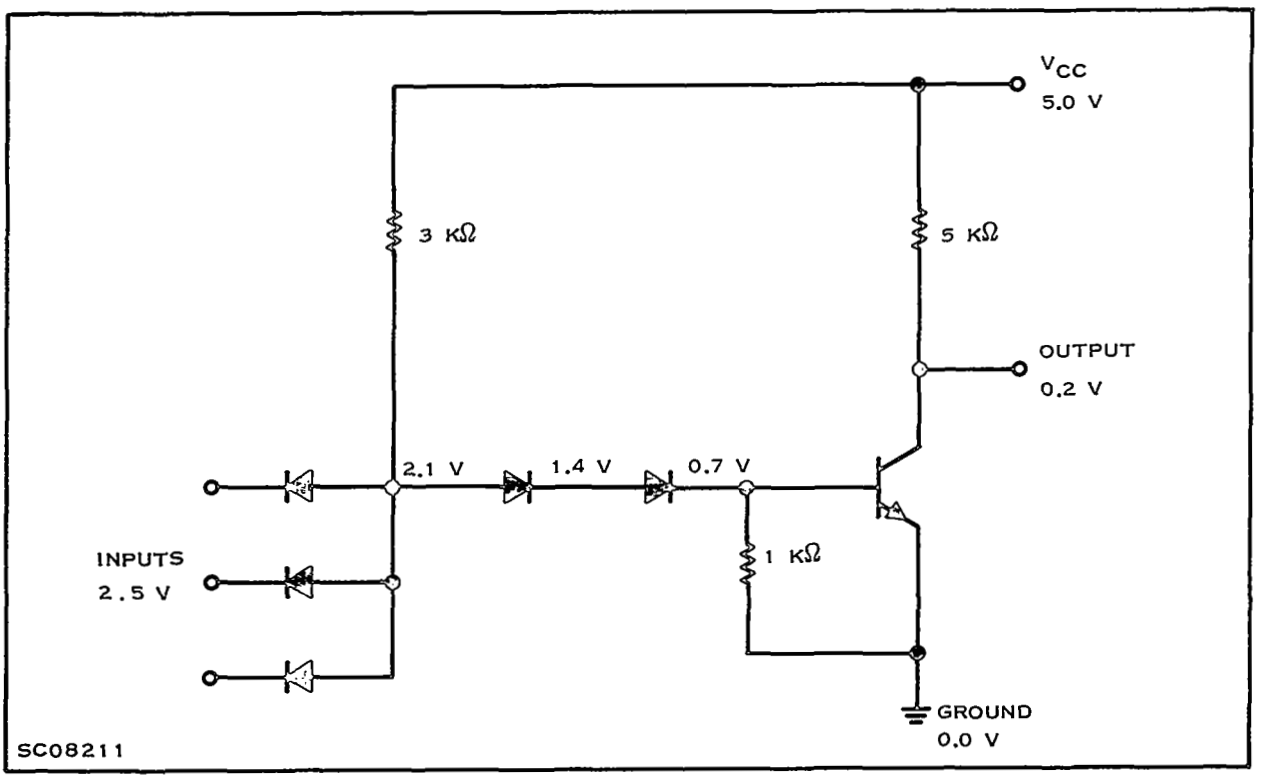


Figure 3-88. Expected Voltage Values of Good DTL Gate

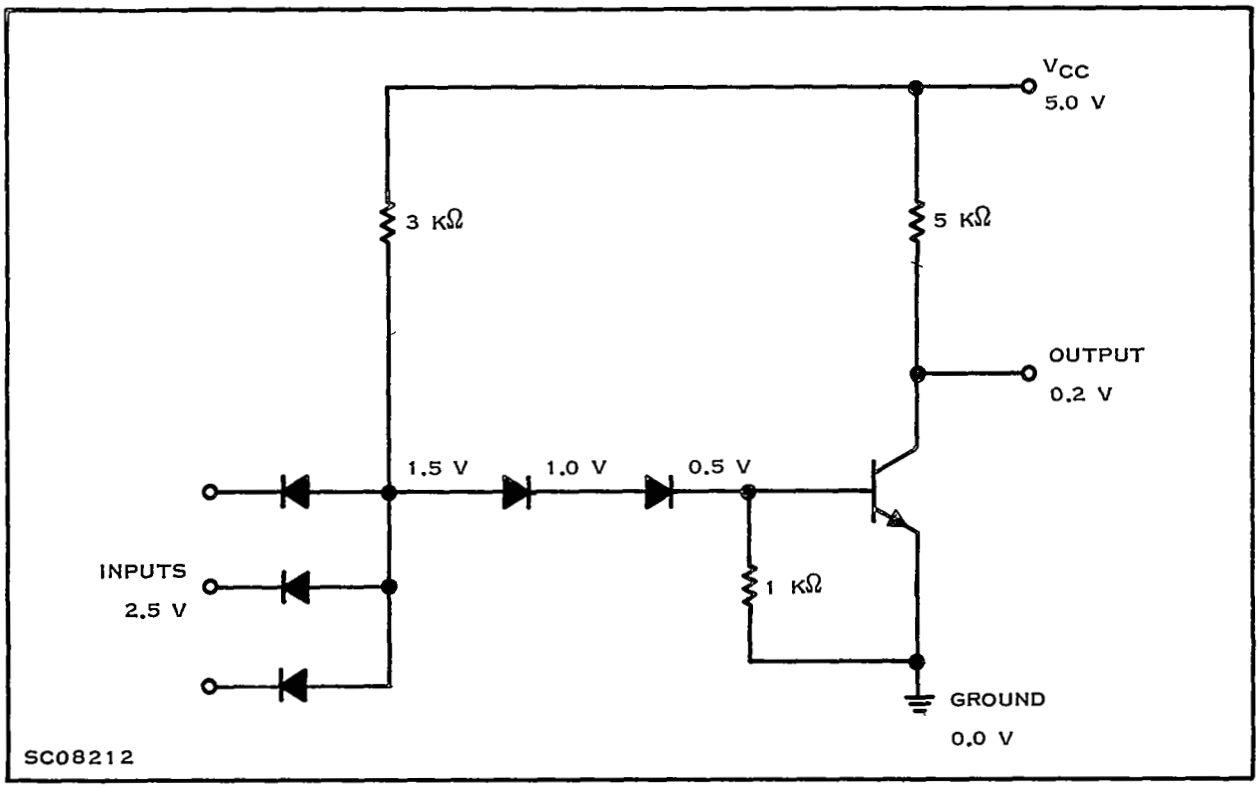


Figure 3-89. Actual Voltage Values of Defective DTL Gate

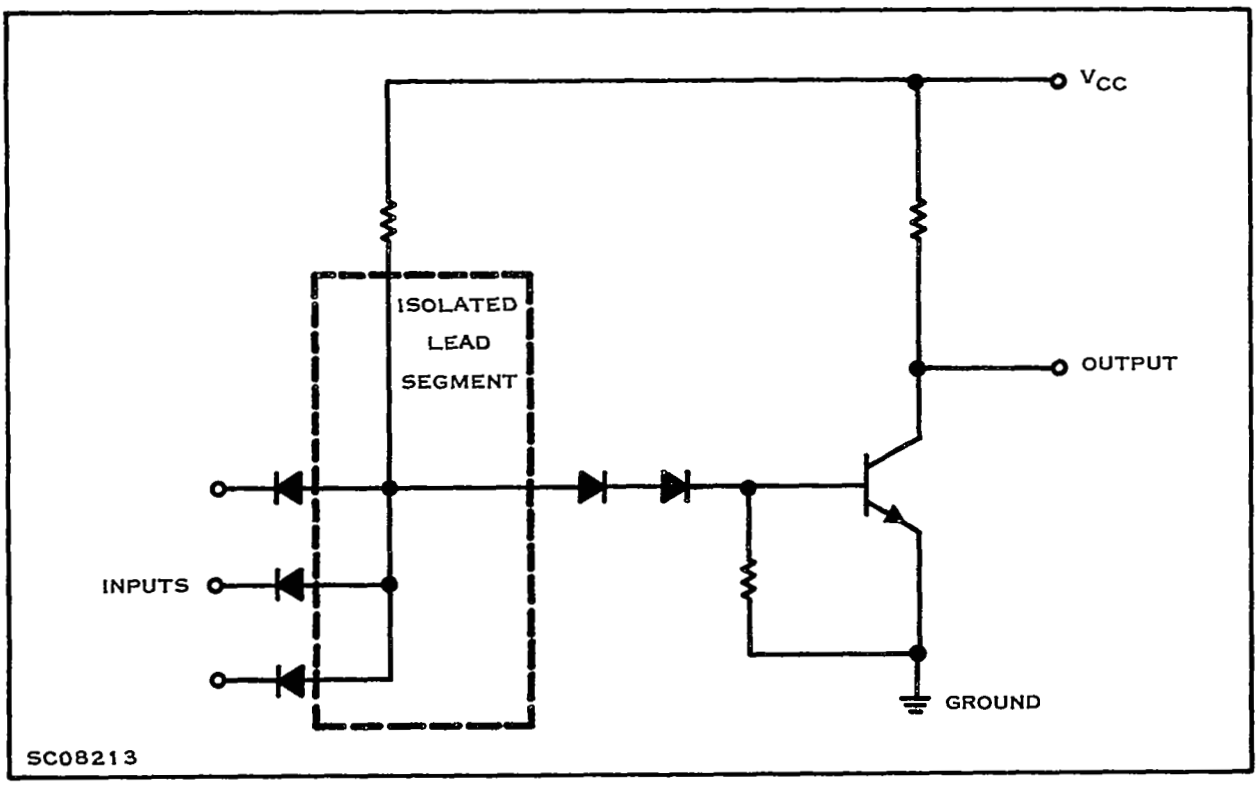


Figure 3-90. Lead Segment Containing DTL Gate Defect

Because of this relationship, most linear circuits are used as amplifiers. (For a discussion of the theory of operation of certain types of linear circuits, refer to Volume 1 of this Handbook.)

b. Direct-Current and Alternating-Current Circuit Analysis

(1). Direct-Current Circuit Analysis. Direct-current circuit analysis will be presented here, and the subject circuit will be the differential amplifier. The schematic for this circuit is shown in Figure 3-91.

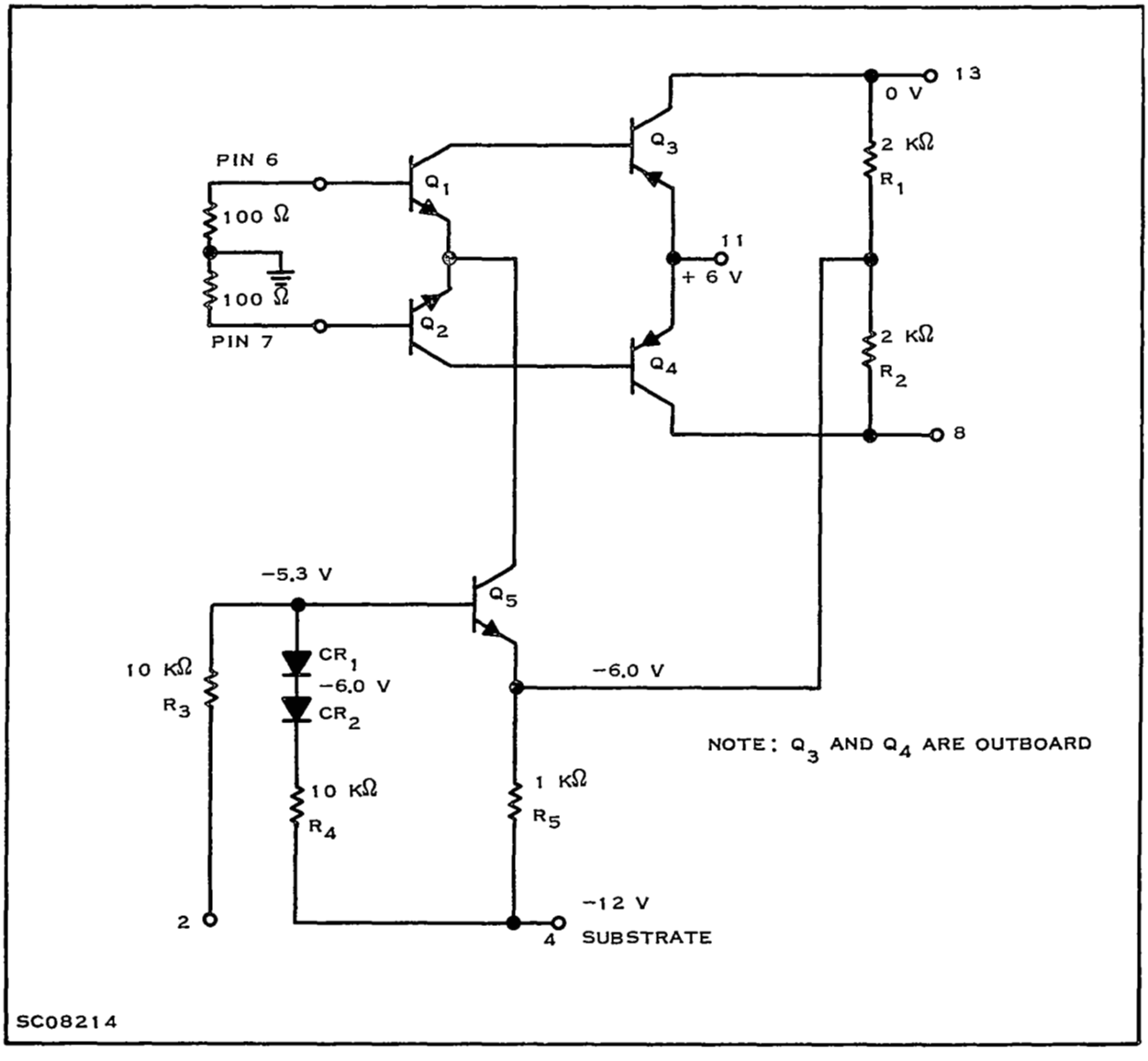


Figure 3-91. Differential Amplifier Circuit (SN350, Texas Instruments)

First the dc bias values must be obtained. The specification for the use of the device provides the starting point. In Figure 3-91, pin 4 (substrate) is biased at −12 V, pin 11 at +6 V, and pin 2 is at ground. Pin 6 and pin 7 are connected to ground through a biasing resistor which provides base current for transistors Q_1 and Q_2. To begin the analysis, consider the divider between pin 2 and pin 4. For the moment, assume that Q_5 is disconnected; then, the voltage at the point between $(CR)_2$ and $(CR)_1$ is −6 V, with 600 μA of current flowing. Assuming that the dc beta (β_{dc}) of Q_5 is 50, the reflected load of the 1-kΩ emitter resistance, R_5, is 50 kΩ. The impedance of the Q_5 emitter-base circuit is high enough, compared to the diode-resistor branch, that the effect on the voltage distribution is negligible for the purposes of this discussion. The voltage at the emitter of Q_5 is, therefore, about −6 V. If it were more negative, more current (amplified by 50 times) would flow in the base. If the voltage were much more positive, Q_5 would become "cut off," allowing no current to flow in the amplifier. Thus, transistor Q_5 forms a constant-current source, with the current through the 1-kΩ resistor being 6 V/1 kΩ or 6 mA.

For good class A operation, the dc voltage at the outputs (pins 13 and 8) must be equal and zero. This means that 3 mA/side must flow through each 2-kΩ resistor. Let us assume that the betas (dc) of Q_3 and Q_4 are each measured at 100. The current flowing in the base of Q_3 and Q_4 is 3 mA/100 or 30 μA. This means that 60 μA must be supplied by Q_5. In order for 30 μA to flow in the collectors of both Q_1 and Q_2, current must exist in both base circuits (pins 6 and 7). If the betas of transistors Q_1 and Q_2 are 50, the base current will be 30 μA/50 or 0.6 μA. This will cause a voltage of near zero at pin 6 and pin 7. Here again, if Q_1 and Q_2 were to draw more emitter current, the voltage at the emitter of Q_5 would cause Q_5 to go toward cut-off, thereby decreasing the currents. Usually, R_5 resistor is constructed with "taps" to permit resistance selection such that the balanced outputs of pins 13 and 8 are near zero. Normally, a balancing circuit is connected to pin 6 and 7 for the purpose of adjusting the dc bias. The object is to cause output voltages of equal value that are very near zero volts. In this discussion, it has been assumed that the circuit is composed of ideally matched elements such that the balancing circuit is not necessary.

The voltage at the common emitters of Q_1 and Q_2 is about one diode-drop negative from ground (−0.7 V). The voltage at the bases of Q_3 and Q_4 is one diode-drop from +6 V (+5.3 volts). This completes the dc analysis. All the currents and voltages are known. This information will allow analysis of any dc failure such as would be evidenced by variations in dc off-set voltages and currents.

(2). Alternating-Current Circuit Analysis

(a). Transistor Operation. In order to analyze ac failures (input impedance, gains, etc.), one must understand the ac characteristics of the circuit. Basic transistor operation will be discussed first, and thereafter ac circuit analysis.

If a transistor's base-emitter junction is back-biased, no current will flow in the collector. The same is true if the base is open circuited. For this case, the transistor is considered to be operating in region I of Figure 3-92 and is said to be "cut-off." 1/ If the emitter-base junction is forward-biased and the collector-base junction is reverse biased, the transistor operation is in region II, the amplification region. This is the region of highest power dissipation. If the base drive (the base current) is increased, the voltage across the collector-emitter junction will decrease, due to the voltage drop across R_L, until the voltage level equal to V_{ce} saturation has been reached. Additional base drive will cause both junctions to be forward-biased, with operation occurring in region III, where the transistor is said to be saturated "on." This discussion of linear circuits will be concerned mainly with transistor operation in region II. When a transistor is biased in region II, an ac equivalent circuit may be drawn as in Figure 3-93, which is one of the most common circuits used. For most of the analysis, this low-frequency circuit will suffice.

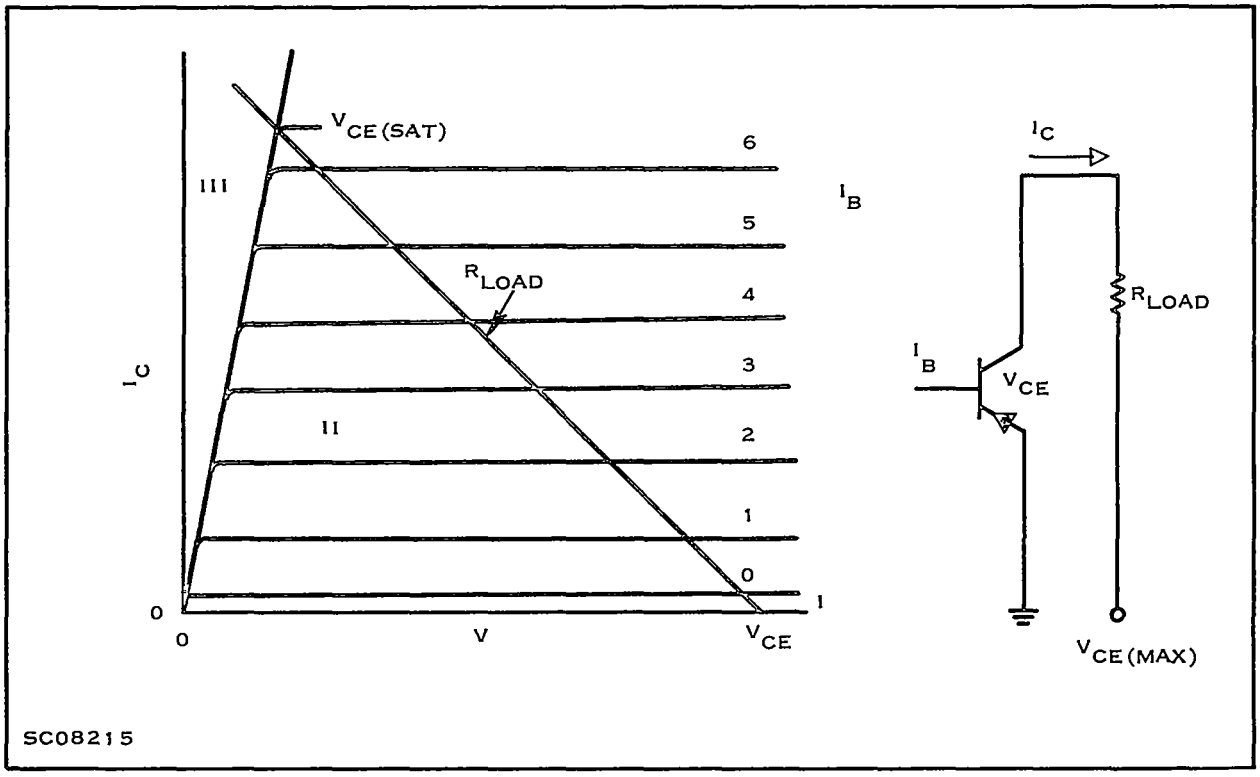


Figure 3-92. Transistor Operating Regions

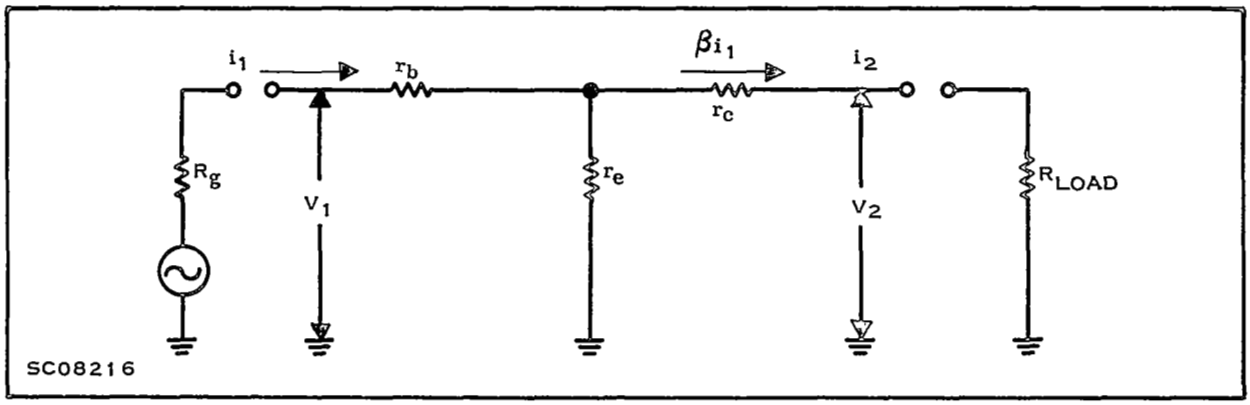


Figure 3-93. Transistor Low-Frequency Equivalent Circuit

(b). Measurement of Alternating-Current Parameters

(1). General. Probably, the best way to measure the ac parameters is to build a dc bias network and an ac bridge circuit. However, such a project is more sophisticated than is required for failure analysis purposes. This discussion is limited to the use of a standard transistor curve tracer. For best results, the parameters discussed here should be measured at the normal circuit operating levels.

(2). Dynamic Emitter Resistance. Dynamic emitter resistance, r_e, is defined as:

$$r_e = \left. \frac{\Delta v_{eb}}{\Delta i_e} \right|_{I_B} \tag{5}$$

where

v_{eb} = emitter-to-base voltage (instantaneous)

i_e = emitter current (instantaneous)

I_B = base current (dc)

The actual values of Δv_{eb} and Δi_e may be read directly from the curve-tracer screen, as shown in Figure 3-94. For a Δv_{eb} of 0.01 V, Δi_e is 13 μA; therefore:

$$r_e = \frac{0.01 \text{ V}}{13 \times 10^{-6} \text{ A}} = 770 \ \Omega$$

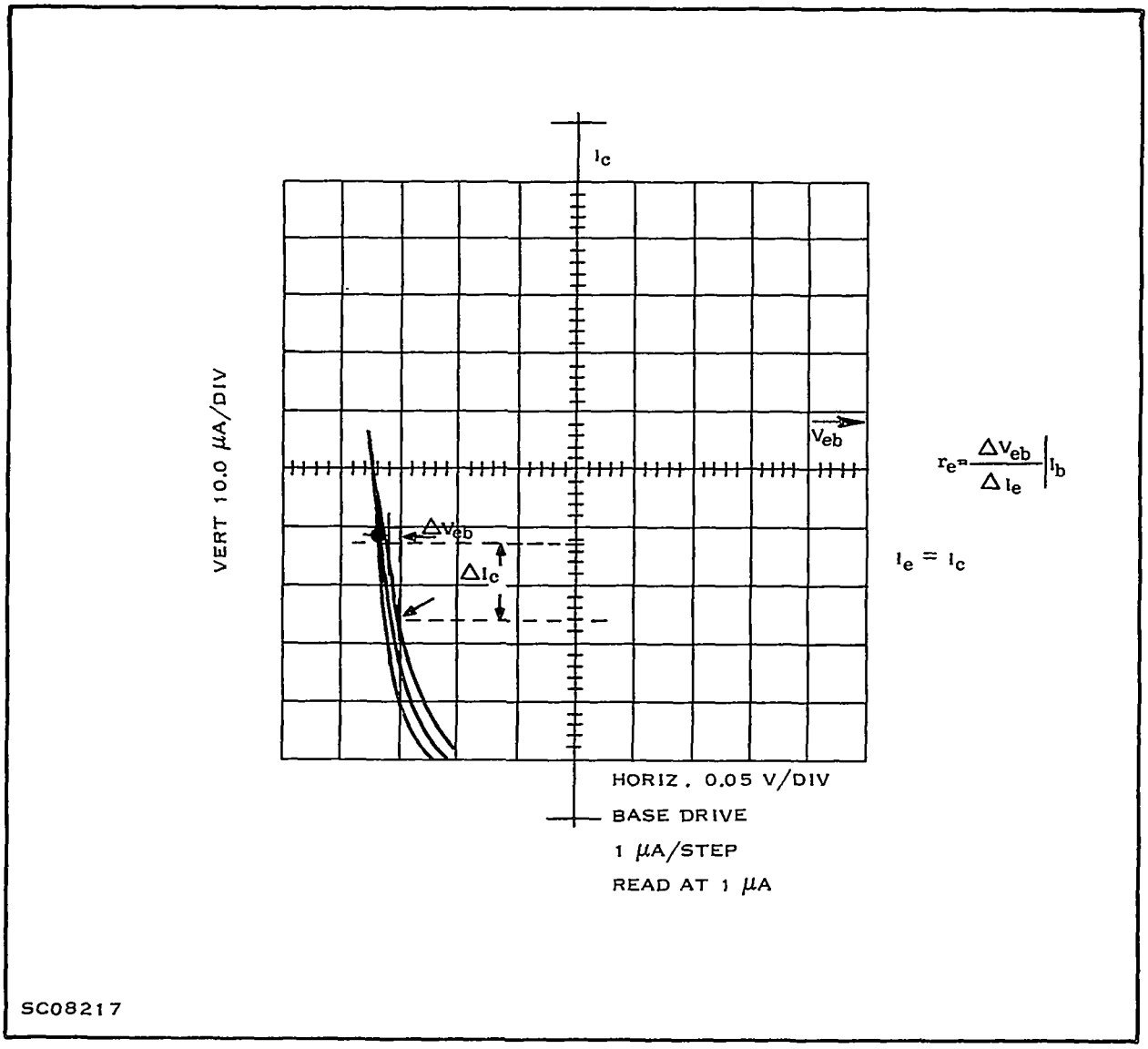


Figure 3-94. Curve Tracer Display for r_e Determination

The transistor's emitter, base and collector are connected to the corresponding curve tracer terminals either by probing or direct pin connection, whichever is appropriate. The curve-tracer's vertical display is set to "collector current," and the horizontal display to "base voltage." The base drive should be set so that ten equal step-adjustments in the base current will result in currents near the normal operating point. The base step polarity depends on the type of transistor under test.

A reasonably accurate method of calculating r_e is available as a substitute for the preceding method. The emitter resistance can be thought of as being made up of two parts:

- The contact and bulk resistance of the emitter.
- The PN junction resistance, r_{PN}, which is a function of the collector current, I_C.

The value of r_{PN} is given by[2/]

$$r_{PN} = \frac{\delta}{I_C} \tag{6}$$

where

I_C = collector current (dc) at saturation

and

$$\delta = \frac{KT}{q} \tag{7}$$

$$= 0.026 \text{ V at } 300°C$$

where

K = Boltzman's constant

T = temperature degrees Kelvin

q = charge on electron

For low-bias transistors, r_e is equal to r_{PN}. This is true at room temperature (27°C). Therefore, by this substitute method:

$$r_e = r_{PN} = \frac{0.026 \text{ V}}{30 \times 10^{-6} \text{ A}} = 866 \ \Omega$$

(3). Dynamic Base Resistance. The dynamic base resistance, r_b, is given by:

$$r_b = \left. \frac{\Delta v_{eb}}{\Delta i_b} \right|_{I_E} \tag{8}$$

where

i_b = base current (instantaneous)

I_E = emitter current (dc) at saturation

The two instantaneous values, Δv_{eb} and Δi_b, may be read directly from the curve-tracer screen, as shown in Figure 3-95. For a Δi_b of 20 μA, Δv_{eb} is 20 mV. Therefore:

$$r_b = \frac{20 \times 10^{-3}\ V}{20 \times 10^{-6}\ A} = 1000\ \Omega$$

For the measurement of Δv_{eb} and Δi_b, the emitter of the transistor should be connected to the curve tracer's base terminal in order to supply a constant emitter current. The transistor base is connected to the curve tracer's emitter terminal. For both measurements, the collector should remain connected to the corresponding CT terminal.

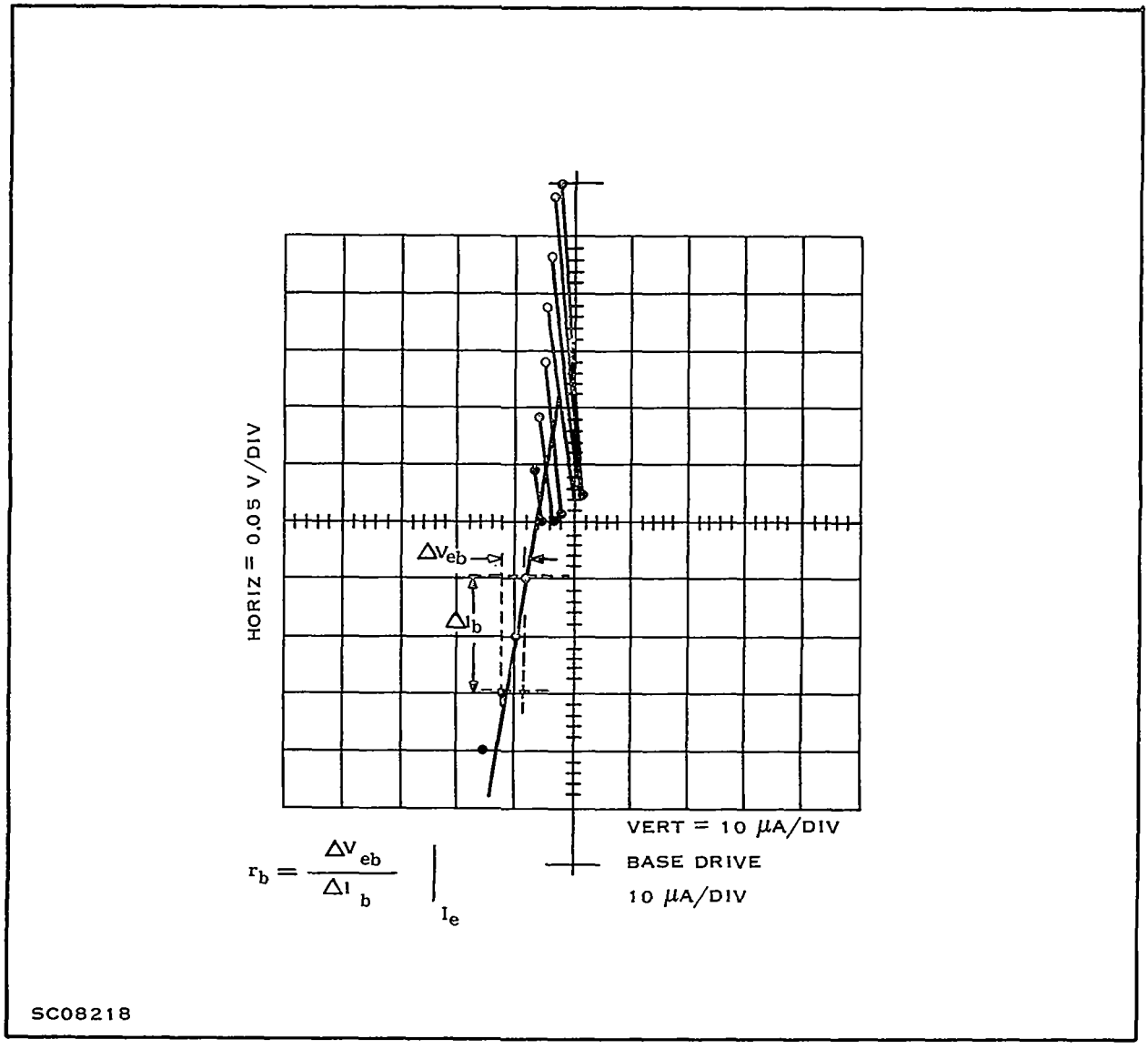


Figure 3-95. Curve Tracer Display for r_b Determination

NOTE

The base step polarity must be reversed from the polarity normally used. The base drive is really the emitter current and should be set near the operating point.

The vertical display and horizontal display remain on "collector current" and "base voltage," respectively.

(4). Current Gain. Current gain, β_{ac}, is defined as:

$$\beta_{ac} = \frac{\Delta i_c}{\Delta i_b} \tag{9}$$

where

i_c = collector current (instantaneous)

i_b = base current (instantaneous); one base-step of base-driving current from curve tracer

The two instantaneous values[3], Δi_c and Δi_b, may be read directly from the curve tracer, as shown in Figure 3-96. Substituting the observed values into Equation (9), β_{ac} is:

$$\beta_{ac} = \frac{95 \times 10^{-6}\ A}{10^{-6}\ A} = 95$$

To obtain the observed values of Δi_c and Δi_b, the transistor's emitter, base and collector are connected to the corresponding curve-tracer terminals. The vertical and horizontal displays are on "collector current" and "collector voltage," respectively.

(5). Dynamic Collector Resistance. The dynamic collector resistance, r_c, is given by:

$$r_c = \frac{\Delta v_{ce}}{\Delta i_c} \cdot \beta_{ac} \tag{10}$$

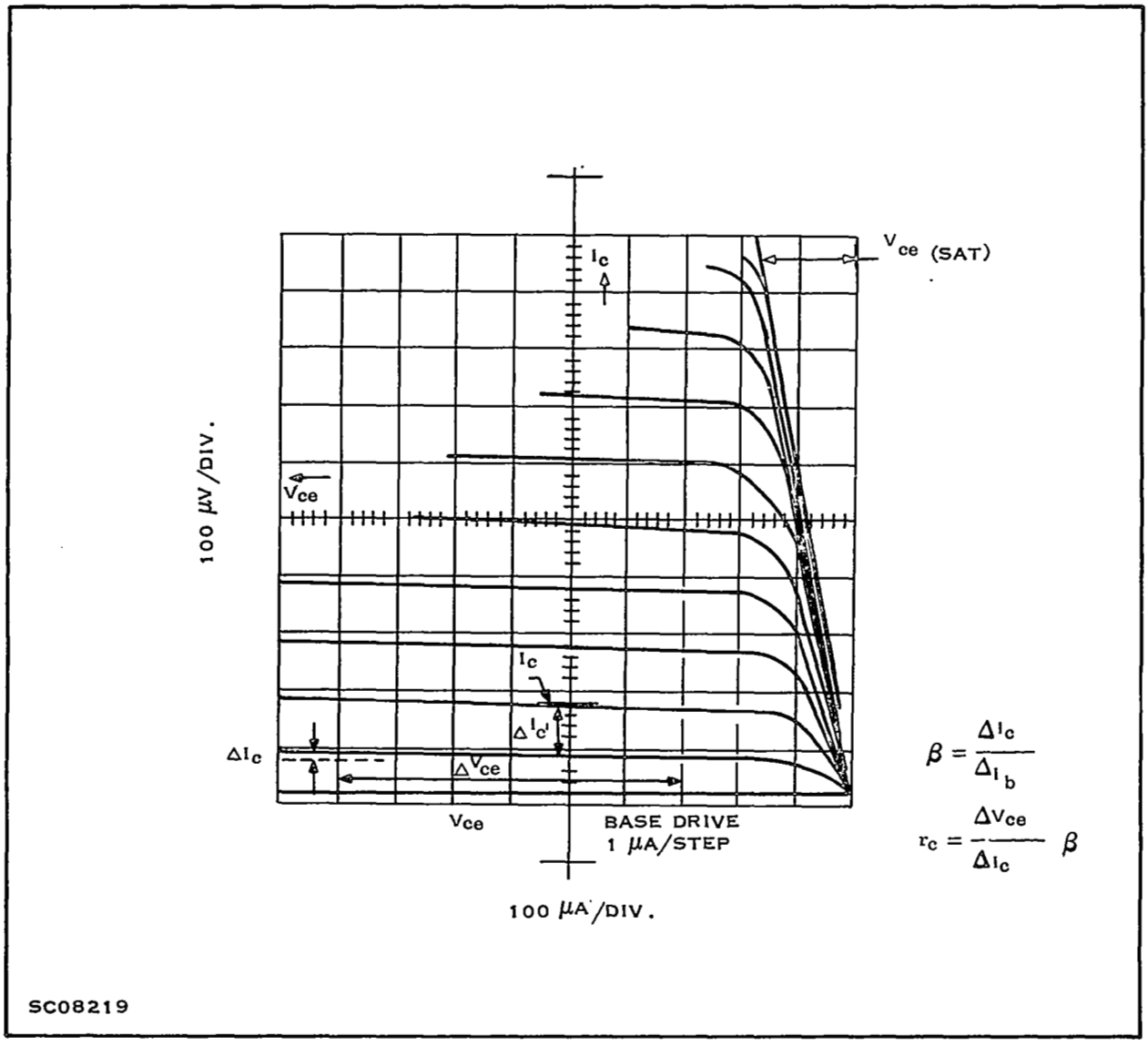


Figure 3-96. Curve Tracer Display for β and r_c Determination

where

v_{ce} = collector-to-emitter voltage (instantaneous)

The values for Δv_{ce} and Δi_c are read directly from the curve tracer, as shown in Figure 3-96. The preceding computation of β was equal to 95. Therefore, in this example the value of the dynamic collector resistance is:

$$r_c = \frac{0.6\ V}{5 \times 10^{-6}\ A} \cdot 95 = 11.4 \times 10^{+6}\ \Omega$$

(3). Measurement of Resistance. Resistance is measured by connecting one side of the resistor to the tracer collector terminal, and the other side of the resistor to the emitter terminal (ground). Care must be taken in all such measurements to exclude parallel elements or parasitic elements. The value of "R" is:

$$R = \frac{\Delta v_{ce}}{\Delta i_c} \tag{11}$$

It is recommended that measurements be made by using a value of voltage that is as near as practical to normal operating voltage. This will be an aid in determining if a resistor is nonlinear. Sometimes, resistor nonlinearity will cause a monolithic microcircuit to fail.

It may not be possible to make measurements at the prevailing current bias without opening contacts. Care should be taken not to open any contacts until the analyst is reasonably certain of the failure mode, since in some cases, this will destroy the unit as far as operation (further electrical analysis) is concerned.

(4). Mathematical Analysis

(a). General. Now that the values for the transistors and resistors are known, one may proceed to mathematically analyze the circuits. A transistor may be connected in three basic connections: common base, common emitter, and common collector, as shown in Figure 3-97(a), (b) and (c). These will be discussed briefly.

(b). Common Base. A common-base-connected circuit is shown in Figure 3-97(a). This configuration has a low input impedance, a high-voltage gain, about unity current gain and a high output impedance.

The derived equations are:

$$Z_{in} = r_e + r_b \cdot \frac{R_L + \frac{r_c}{\beta}}{R_L + r_c + r_b} \tag{12}$$

$$Z_{in} \approx r_e + \frac{r_b}{\beta} \approx r_e$$

where

Z_{in} = input impedance

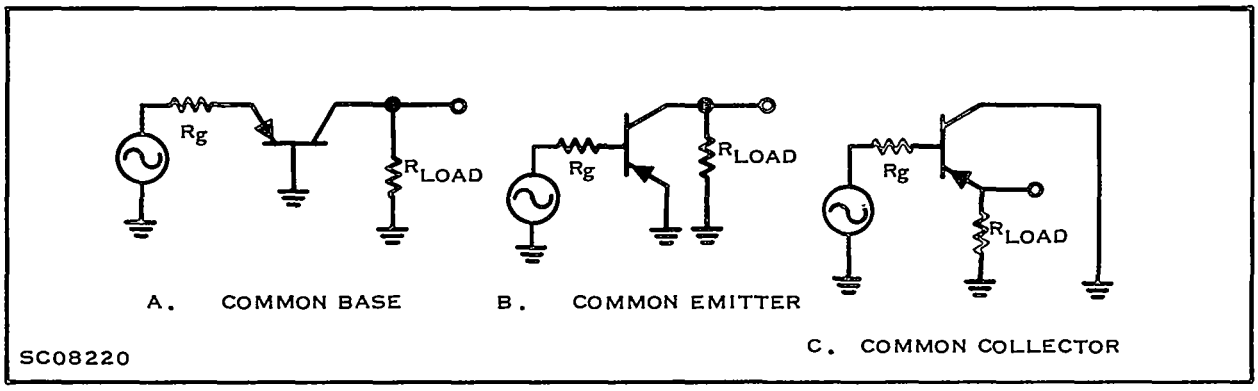


Figure 3-97. Basic Transistor Connections

$$Z_{out} = r_c + r_b \cdot \frac{-r_c + r_e + R_g}{R_g + r_e + r_b} \tag{13}$$

$$Z_{out} \approx r_c \left(1 - \frac{r_b}{R_g + r_e + r_b} \right)$$

where

Z_{out} = output impedance

R_g = generator impedance

$$A_i = \frac{r_b + \alpha r_c}{R_L + r_c + r_b} \tag{14}$$

$$A_i \approx \alpha$$

where

A_i = current gain

$$\alpha = \frac{\beta - 1}{\beta} \tag{15}$$

$$A_v = \frac{R_L\left(r_b + r_c\right)}{r_b\left(R_L + \frac{r_c}{\beta}\right) + r_e\left(R_L + r_c + r_b\right)} \tag{16}$$

$$A_v \approx \frac{R_L}{r_e}$$

where

A_v = voltage gain

It should be noted that the term "α" was not used in most of the equations, since its deletion introduces no more than a five percent error. The common-base configuration is not commonly used.

(c). Common Emitter. The common-emitter connection has a medium input impedance and a medium output impedance. The circuit is shown in Figure 3-97(b). Due to the fact that the load impedance should match the output impedance, this configuration will have a medium-to-high voltage gain. The current gain also is medium-to-high. The derived equations are:

$$Z_{in} = r_b + \frac{r_e\left(R_L + r_c\right)}{R_L + \frac{r_c}{\beta} + r_e} \tag{17}$$

$$Z_{in} \approx r_b + \frac{\beta r_e r_c}{\beta r_e + r_c}$$

$$Z_{out} = \frac{r_c}{\beta} + \frac{r_e\left(R_g + r_b + r_c\right)}{R_g + r_b + r_e} \tag{18}$$

$$Z_{out} \approx \frac{r_c}{\beta} + \frac{r_e r_c}{R_g + r_b + r_e}$$

$$A_i = \frac{r_c - r_e}{R_L + r_e + \frac{r_c}{\beta}} \tag{19}$$

$$A_i \approx \beta$$

$$A_v = \frac{-R_L\left(r_c - r_e\right)}{r_e\left(R_L + r_c\right) + r_b\left(R_L + \frac{r_c}{\beta} + r_e\right)} \tag{20}$$

$$A_v \approx \frac{R_L}{r_e}$$

In the preceding equations, (17) through (20), the term "r_e" contains any "feedback" resistance in the emitter circuit. Of the three common connections, this circuit is the most versatile arrangement and is most commonly used.

(d). Common Collector. The common collector or emitter follower circuit (Figure 3-97 "c") has no phase inversions, has a high current gain, a voltage gain of near unity, a high input impedance and a low output impedance. The equations to be used in the analysis of this circuit are:

$$Z_{in} = r_b + \frac{r_c\left(R_L + r_e\right)}{R_L + r_e + \frac{r_c}{\beta}} \tag{21}$$

$$\approx r_b + \beta\left(R_L + r_e\right)$$

$$Z_{out} = r_e + \frac{\frac{r_c}{\beta}\left(R_g + r_b\right)}{R_g + r_b + r_c} \tag{22}$$

$$\approx r_e + \frac{R_g + r_b}{\beta}$$

$$A_i = \frac{r_c}{R_L + r_e + \frac{r_c}{\beta}} \tag{23}$$

$$\approx \beta$$

$$A_v = \frac{r_c R_L}{r_b\left(R_L + r_e + \frac{r_c}{\beta}\right) + r_c\left(R_L + r_e\right)} \tag{24}$$

$$\approx \frac{R_L}{\frac{r_b}{\beta} + R_L} \approx 1$$

This circuit is useful as an output stage for a preamplifier, for the condition where long cables are to be connected. A two-transistor connection in which the common collector and the emitter of the first transistor feed the

base of the second transistor is known as a Darlington pair, which has a combined β of $\beta_1 \cdot \beta_2$. This allows an extremely high input impedance for a very low output impedance load.

The preceding equations were derived from the matrix equation for a three-port device. Care should be taken to insure that the given equations are altered correctly for a given circuit containing feedback elements.

(5). An Example of Alternating-Current Circuit Analysis. For this example of how to identify the cause of failure of an ac circuit, the circuit shown in Figure 3-98 will be used to demonstrate the procedures of ac analysis. (For simplification, transistor Q_4, similar to Q_3 and shown in Figure 3-91, is not shown in Figure 3-98.

With a signal applied to transistor Q_1, the stage containing transistor Q_2 will be operated as a common-base connection. Examination of the equation for the input impedance of a common-base connection, Equation (12), will show that Z_{in} is nearly equal to the dynamic emitter resistance, r_e. Further along in this analysis it will be shown that the load resistance, R_L, for Q_1 and Q_2 is about 1 kΩ. For the condition of a low current level, the r_e of Q_2 is about 866 Ω (this resistance can be measured by the procedure described earlier). The Z_{in} of Q_1 can be computed by using Equation (17). In this example, r_e is equal to $r_e\, Q_1 + Z_{in}\, Q_2$, or almost 2 r_e (matched Q_1 and Q_2). Since r_c is much larger than $\beta\, r_e$ (r_e is about 15 MΩ), $Z_{in}\, Q_1 = r_b + \beta R_e \approx \beta R_e$, but $R_e = 2\, r_e\, Q_1$. Therefore, $Z_{in}\, Q_1 = 2\, \beta\, r_e\, Q_1 = 2 \cdot 50 \cdot 866 =$ 86.6 kΩ. With no load on the output, R_L is just 2 kΩ for Q_3. Since this circuit is also a common-emitter connection, $Z_{in}\, Q_3 = \beta\, r_e\, Q_3$ per stage, at a collector current of 3 mA. The value of r_e, 10 Ω, is expected to be lower for Q_3 than for Q_1. Therefore, $Z_{in}\, Q_3 = \beta\, Q_3 = 100 \cdot 10 = 1.0$ kΩ. (The Q_4 portion of the circuit shown in Figure 3-91 may be analyzed in the same manner as has been presented here for Q_3 shown in Figure 3-98.

At this point, the loading effect of Q_5 may be questioned. Transistor Q_5 is shown in Figure 3-98 as a common-emitter connection, with no signal (matched operation) on either the base or the emitter. For the common-emitter connection,

$$Z_{out} = \frac{r_c}{\beta} + \frac{r_e\, r_c}{R_g + r_b + r_e} \cdot \qquad (18)$$

In this example, Z_{out} is about 500 k Ω, which is high enough in comparison to 866 Ω (the r_e of Q_2) that it may be ignored.

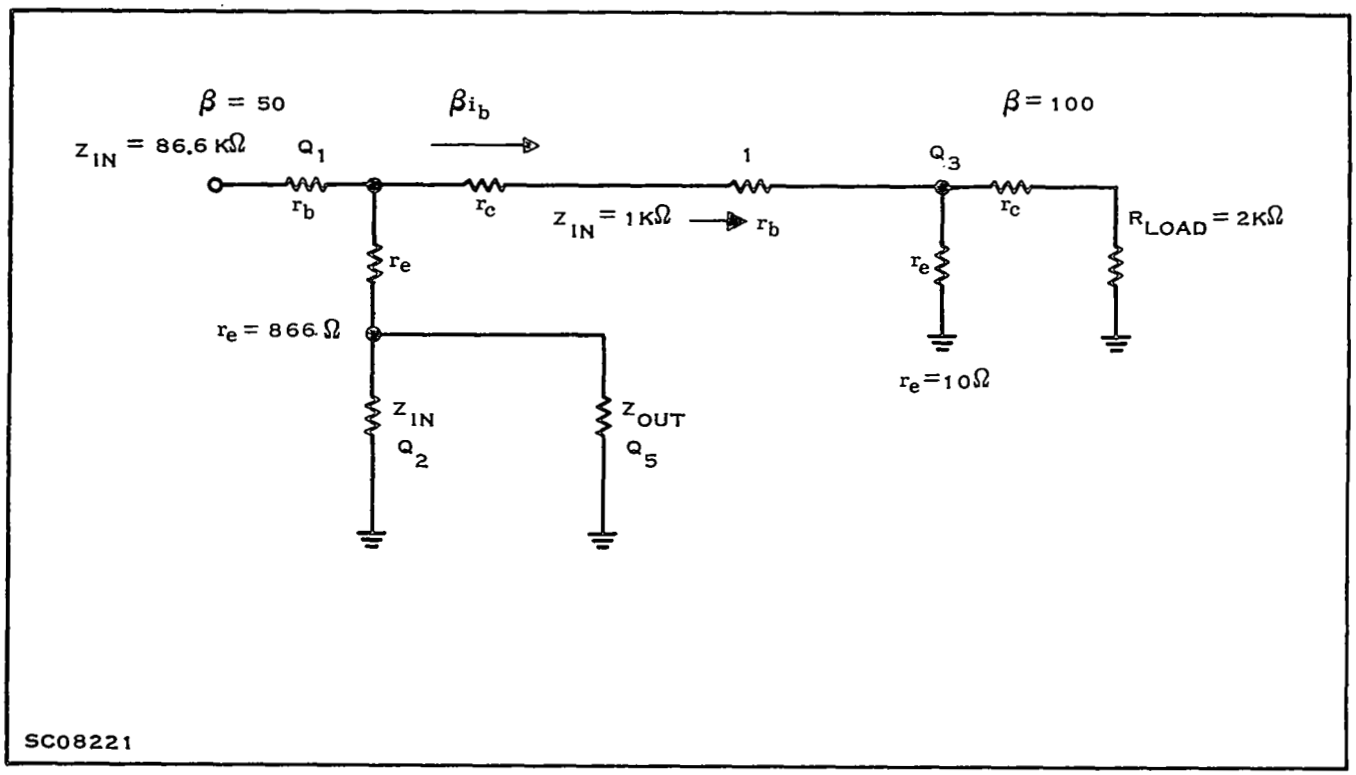


Figure 3-98. Equivalent Circuit of SN350 Differential Amplifier

Now that the input impedance has been determined, the gains may be calculated. Using the voltage gain equation for the common emitter connection, the voltage gain for the output-stage side of the circuit is:

$$A_{v(output)} \approx \frac{R_L}{r_e} = \frac{2\ k\Omega}{10\ \Omega} = 200 \qquad (16),(20)$$

In the same way, the gain for the input stages (both common base and common emitter) is:

$$A_{v(input)} \approx \frac{R_L}{2\ r_e} \qquad (25)$$

$$= \frac{1.0\ k\Omega}{2 \cdot 866} = 0.57$$

The gain for one side of the amplifier is:

$$A_{v(one\ side)} = A_{v(input)} \cdot A_{v(output)} \qquad (26)$$

$$= 0.57 \cdot 200 = 165.0$$

Thus the gain for both sides (and the overall gain of the unit) would be:

$$A_{v(total)} = 2 \cdot A_{v(one\ side)}$$

$$= 2 \cdot 165.0 = 330.0$$

Further analysis would include the calculation of output impedance, Z_{out}, the amount of feedback, or the more complex relationships of common mode operation, all of which exceed the scope of this example.

(6). Summary. Summarizing the procedures for performing a failure analysis of a dc or an ac circuit, the circuit is first analyzed for dc bias conditions. Known input and output conditions and power supply voltages are converted to voltages and currents at each node by using Ohm's law and allocating 0.7 V for diode drops. After the dc bias conditions have been computed, measurements are made to determine the various ac parameters of the elements in the circuit, at the correct bias levels. These measured values are then used to calculate the ac parameters of the complete device. From these calculations, the important factors governing the operation of the parameter that failed can be determined. As an example of how useful the knowledge of an important fact about a parameter can be in a failure analysis, if the failed circuit is a common emitter amplifier, β will not affect the voltage gain of the stage but will affect the voltage gain of the preceding stage, through the reflected load.

c. Visual Verification of Defects

(1). General. Visual inspection often reveals a number of abnormal conditions which may or may not cause electrical failure. It must be determined if the condition is causing the observed electrical problem. This discussion will present methods for such a determination.

(2). Open Circuits. One of the common electrical conditions which occurs is an open circuit. The visual indications of an open circuit may consist of one of the following conditions:

- Scratched metallization
- Peeled metallization
- Chemical decomposition
- Lifted bonds
- Broken wires
- Open stitch bonds
- Melted leads
- Cracked bars.

The obvious method of determining if an observed open condition is causing the electrical parameter to be bad is to use a probe to close the open or patch it with conductive epoxy.

Sometimes, damage is observed, but it is not visually obvious that an electrical open exists. This commonly occurs with scratches, cracked bars and chemical decomposition. A curve-tracer continuity test is recommended for such cases.

Melted leads are occasionally encountered. The analyst is expected to determine why melting occurred. To test the possibility of a device defect, the open or opens are closed by probing or patching while parameter testing is performed. Additional melting indicates a device defect. Proper operation tends to indicate electrical overstress. Linear circuits sometimes contain intentional melting. Factory adjustment of resistance is accomplished in this manner to obtain optimum operational characteristics.

In summary: it should not be assumed that an open condition has caused a particular parameter to fail, since the portion of the circuit in which the open occurs may not be used for that particular parameter. Electrical testing is required for positive determination.

(3). Shorted Circuits. Another common electrical condition is a short. This may result from smeared metallization that has caused shorting of two adjacent leads. It can result from a misplaced ball bond that is shorting two leads. The edge of the bar normally does not contain an oxide layer; therefore, a bond placed near the edge can come in contact with the bare silicon, causing one or more circuits to short to substrate. An oxide defect may allow metallization to short to underlying silicon material. Foreign material or incompletely removed metallization may cause shorts between adjacent leads. Sagging wires may short the circuit to the edge of the bar or to adjacent wires. Flash-across shorts frequently cause a shorted condition to exist across a junction, possibly the emitter-collector junction. A bar improperly placed in the package may be contacting one of the external pins, thus causing a short.

A curve-tracer test to determine if the shorted condition exists is the best method of attack. Assuming that the short does exist, a photograph should be taken to record the actual condition, and if possible, the short should be removed so that a remeasurement of the parameter can be made. A normal parameter reading after the short has been removed indicates that the short was the actual cause of failure. If it is not feasible to remove the short from the circuit, the analyst may resort to circuit analysis to determine if the short could cause the particular parameter to be out of specification.

In other words, the visual appearance of a short may be verified electrically by:

- Curve-tracer measurement
- Removal of the short and parameter remeasurement
- Circuit analysis.

(4). Breakdown Voltage. A number of visual defects can cause an electrical condition known as low-breakdown voltage. Those visual conditions which can be associated with this electrical condition are cracked bars, masking defects, mask misalignment problems, oxide defects and metallization-silicon eutectic formation. To determine if the defect is causing failure, the analyst must determine three things:

- What is normal breakdown voltage?
- What is the maximum voltage which will occur at that point during normal circuit operation?
- What is the actual breakdown voltage at the defect in question?

The normal breakdown voltage may be determined by curve-tracer tests on a "good" microcircuit or a "good" portion of the microcircuit under test. The voltage during normal circuit operation must be determined from an analysis of the circuit operation. The actual breakdown voltage can be obtained from a curve-tracer measurement of the area in question. If the actual breakdown voltage is lower than both the normal value and the value occurring during circuit operation, then it is reasonable to assume that it is detrimental to circuit operation. An analysis of the particular parameter which has failed will indicate whether or not it was caused by the low breakdown.

d. Determining Nonobserved Defects

(1). General. The first objective in determining the location of nonobserved defects is to find the area or circuit in which the defect is located. One method of accomplishing this objective is to compare electrical characteristics of the defective device with known normal electrical characteristics. The normal electrical data may be obtained by either a mathematical analysis or probing of a good device. Defective device characteristics are best obtained by probing while the device is connected for failed parameter testing. The defective area or circuit is likely to exist where the electrical characteristics depart from the normal operating range. In some cases, such as an opening in the oxide under an evaporated lead, this defect is also visible. Sometimes, as with high or low betas, it is not visible. The defect, when

necessary, is isolated by opening leads to the element in question. The curve tracer or electrometer is useful to determine the exact location of the defect. It may be advantageous to substitute exterior elements (resistors, etc.) by "probing" the elements into the circuit. The operation of the circuit can then be checked and the failed element verified as the cause of failure.

(2). Direct-Current Circuit-Failure Analysis

(a). General. Abnormally high power-supply currents are occasionally encountered. Several things which may affect the amount of power-supply current are exceedingly low beta, low resistance values, or leakage paths. In the case of low beta, more base drive will be needed to maintain the collector current needed for operation. If this is the case for an interior or output stage, the currents must be supplied through a preceeding stage, and hence, from a power supply. A more common cause of excessive power-supply current is due to reduced resistance values, since many units are designed such that output voltage levels are maintained regardless of the resistance values. Leakage paths may be caused by oxide defects, inversions, or improper diffusions which allow direct power-supply current to substrate or ground.

A number of problems are occasionally encountered which pertain to the input and output dc offset voltages. This can manifest itself in a failure of the unit to balance properly, to have out-of-specification values of either the parameter called differential input voltage offset (DIVO) or the output parameter called common mode output voltage offset (CMOVO) or both. The inability to balance (output voltages cannot be adjusted to be equal to each other) can be caused by low, high or mismatched betas, or by excess leakages caused by oxide defects, etc. Insufficient resistance values can also cause these problems.

(b). An Example of Direct-Current Circuit-Failure Analysis. An example of dc circuit-failure analysis will be illustrated by describing the methods that were used to successfully analyze and identify the condition which caused a differential amplifier to operate in an abnormal manner. The amplifier's schematic is shown in Figure 3-99. The failed parameters were:

- Higher than normal power-supply currents at pins 4 and 11.
- Output pins 8 and 13: offset voltage higher than its normal value of 330 mV, and positive. This parameter, common mode output voltage offset (CMOVO), is measured when the outputs are equal (balanced condition).
- Other dc and ac parameters were abnormal but were not significantly useful for this analysis.

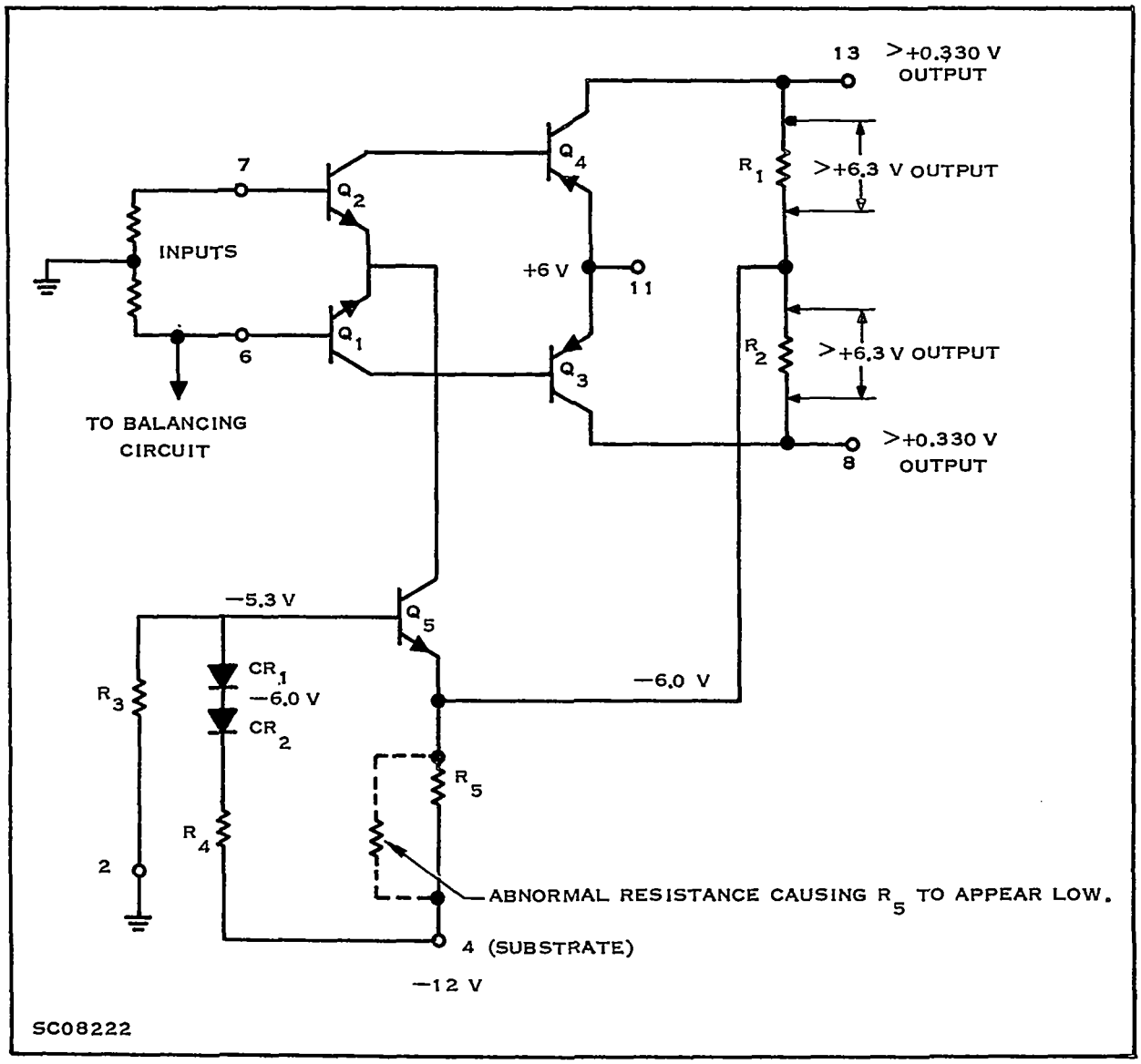


Figure 3-99. Actual Voltage Values of Defective SN350 Differential Amplifier

In order to find the failure-causing condition, voltage and resistance tests were made. The emitter voltage of transistor Q_5 is a very important test point; it measured normal at approximately −6.0 V. This indicated that Q_5 and the bias network attached to the Q_5 base were good. However, it also indicated that the voltage drop across resistors R_1 and R_2, in Figure 3-99, was greater than 6.3 V, an above normal value. The analyst concluded from this information that either R_1 and R_2 were high in value or R_5 was low. A curve-tracer test of the resistances quickly revealed that R_5 was low.

Next, R_5 was investigated to determine, if possible, why it measured 800 Ω instead of 1 k Ω. Isolation of R_5 from the remainder of the circuit, by opening the metallization at both ends, was required. With R_5 isolated, it now equaled 1000 ohms, its normal value. Measurement between R_5 and substrate (pin 4) revealed a resistive connection where none should exist. A planar metallurgical (horizontal) section, followed by staining, revealed a resistive path through, and due to, an improper diffusion between resistor R_5 and substrate. An illustration showing a typical example of this type of defect will be presented later.

The probable manner in which certain of the device's parameters failed is relatively simple to describe. The emitter of transistor Q_5 is normally locked at −6 V by its bias circuit. If R_5 is reduced in value, more current is required to maintain the 6-V drop across R_5. Part of this increased current will exist in Q_5, which, obviously, is turned "on" harder. The increased current of Q_5 proceeds through Q_1 and Q_2, requiring additional base drive through input pins 6 and 7. The base currents of transistors Q_3 and Q_4 are increased as a result, causing both to turn "on" more. Thus the collector resistors of Q_3 and Q_4 must carry more current and drop more voltage, which causes CMOVO to increase in the positive direction. Power supply currents must also increase.

(3). Alternating-Current Circuit-Failure Analysis

(a). General. A determination of the conditions causing ac parameter failures is more difficult than was the case with dc. Small capacitance or resistance problems which do not affect dc parameters may affect ac parameters. A discussion of the conditions causing ac parameter failures will be presented here.

(b). Alternating-Current Parameter Failures

(1). Gain. The gains of series stages multiply. If the gains are as shown in Figure 3-100, then the overall gain will be

$$A_v = A_{v1} \cdot A_{v2} \tag{27}$$

where

A_{v1} = voltage gain of first stage

A_{v2} = voltage gain of second stage

In a differential amplifier such as that of Figure 3-91 which is simplified in Figure 3-101, the gains of the two parallel paths add as follows:

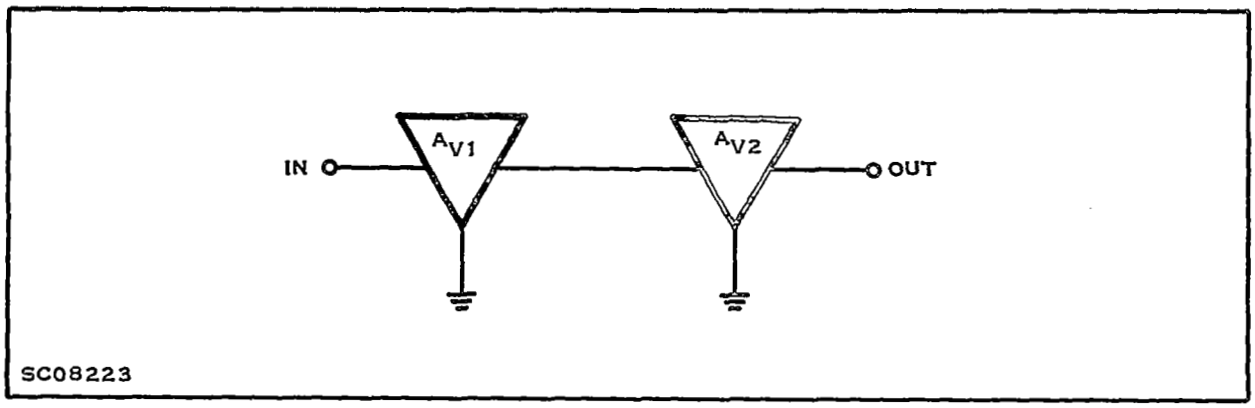


Figure 3-100. Gains of Series Stages Multiply ($A_{v1} \cdot A_{v2}$)

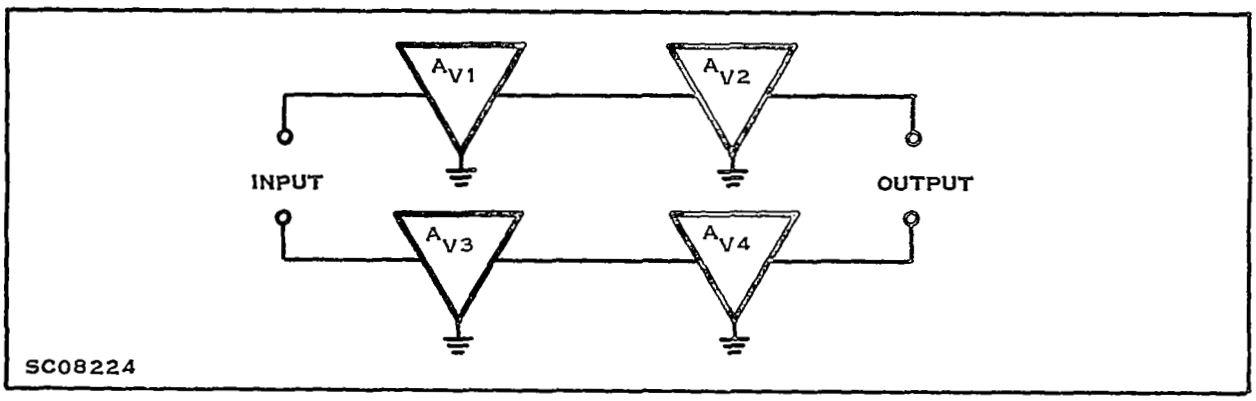


Figure 3-101. Simplified Form of SN350 Differential Amplifier Circuit

$$A_v = \frac{\text{output}}{\text{input}} = A_{v1} \cdot A_{v2} + A_{v3} \cdot A_{v4} \qquad (28)$$

Understandably, the cause of low gain is a low gain in one or more of the stages. The direct cause of loss of gain will not be β, as a rule, since the gain is:

$$A_v \approx \frac{R_L}{r_e} \qquad (16),(20)$$

If the value of r_e on a grounded base or emitter is large (usually accompanied by a low β), the gain of that stage will be low. The R_L for the preceeding stage is β (r_e) for the stage in question, and unless the increase in r_e offsets a low β, the gain will be low. Of course, oxide defects allow extra loading, and improper load resistors will also affect the gains.

(2). Input-Output Impedance. Both input and output impedance are functions of a transistor's parameters. For the input case, the input impedance is a function of r_e, and the following conditions will apply:

- Collector resistance may enter the picture if extremely high.
- Low values of β or r_e will cause low input impedance.
- The base resistance is a series function.

The output impedance is also a function of the transistor parameters but is affected by R_g, the generator resistance. Therefore, a check of the preceeding stage's output impedance is important. Remember that the equations assume that the output does not include any biasing load resistors. Here again, pinholes and off-value resistors can affect the impedances.

(3). Frequency Response. A failure in frequency response is difficult to analyze. Usually the failure is due to thin oxide which allows the lead pattern to be excessively coupled to the underlying elements. Other defects, such as elements being coupled together due to mask misalignments or diffusion errors may cause the frequency to roll-off too soon. Excessive phase shift due to the capacitance of transistors or other elements may cause this problem. The value of the voltage gain-bandwidth product may be useful in analyzing frequency response. The gain-bandwidth product for a linear unit should be essentially constant. If some element should change its characteristics, thereby causing a gain increase, the bandwidth will decrease.

(4). Common Mode Rejection Ratios. The common mode rejection ratio is the ratio of the normal differential amplifier gain to that with equal inputs. With normal differential operation, the feedback (emitter) resistance is small (ranging from a few ohms to several thousand ohms) and determines the gain of the amplifier. For the common-mode operation, the value of this feedback resistance is much higher (in the megohms for the example given). This will cause a smaller gain, probably less than one. If the value of the input signals to the units are not equal due to poor lead contacts, or if the equivalent common-emitter resistance is low, the common-mode gain will be high.

(5). Output Distortions. Clipping is the cause of most output distortions, due to nonlinearity of the circuit over large signal swings. Usually the cause of failure is an improper load line (due to high- or low-load resistance) or a shift in the bias point due to a change in either the base drive or value of beta. Another cause could be excessive V_{ce} saturation voltage. This usually will show up as a dc-offset voltage problem.

Output distortion or any one of the other four previously mentioned parameters may also fail due to a temperature-voltage inversion, which is discussed later.

(6). Surface-Recombination Effect on Transistor Gain. Transistor gain values are drastically affected by changes in surface recombination characteristics. Evaluation is possible by "low-level" forward current measurements.[4,5] The "low-level" forward current of a P-N junction may be expressed by:

$$I = A\,\epsilon^{\frac{qV}{mKT}} \tag{29}$$

where

A = constant

ϵ = exponential

m = slope of the "low-level" forward current V-I characteristic plotted logarithmically

V = applied base-emitter voltage

q = charge on electron

K = Boltzman's constant

T = temperature degrees Kelvin

The V-I characteristic is measured and plotted in the ranges of 0.25 V to 0.60 V and 10^{-11} A to 10^{-6} A, for both the emitter-base and collector-base junctions.

The mechanism of conduction is determined by m, the slope of the V-I line, in accordance with the following values:

Range of "m" values	Condition
$0.5 \leq m < 1.5$	Normal
$1.5 \leq m < 2.0$	High surface recombination exists
$2.0 \leq m$	Electron channeling is present

An "m" value above 1.5 will be found in conjunction with lower than normal gain, if the degradation is due to surface recombination changes.

5. Examples of Electrical Problems

a. General

The remainder of this discussion on evaluating the device after its package has been opened, describes certain conditions which are frequently observed and discovered by means of an electrical evaluation of the monolithic microcircuit. Many of the conditions are shown in photographs in which the problem area has been indicated. The electrical effects which are normally observed with these conditions, methods of discovering the conditions and the causes of the conditions are discussed.

b. Oxide in Windows

Silicon dioxide sometimes is found in areas intended as low resistance contacts between metallization and silicon material. This condition is known as oxide in windows and is illustrated in color by Figure 3-102. The large rectangular area labeled "No. 1" in Figure 3-103 is partially covered with a blue-appearing oxide layer. The four smaller areas surrounding area "No. 1" have varying shades of blue, indicating varying thicknesses of oxide. The element used in this example is the clock capacitor for a flip-flop circuit.

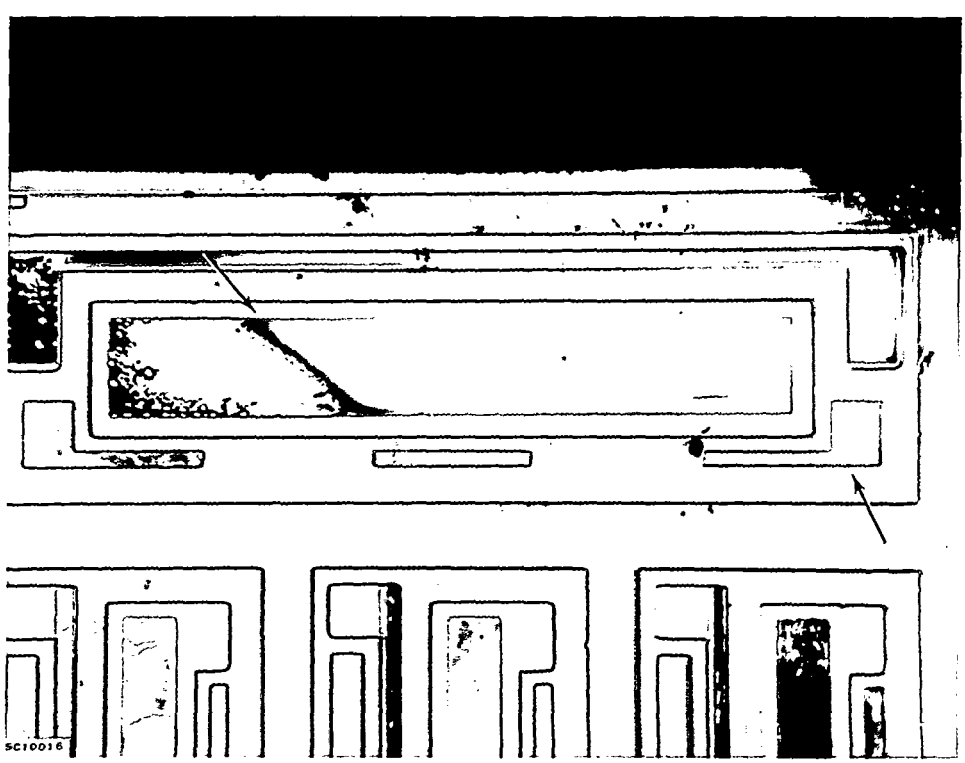


Figure 3-102. Oxide in Windows

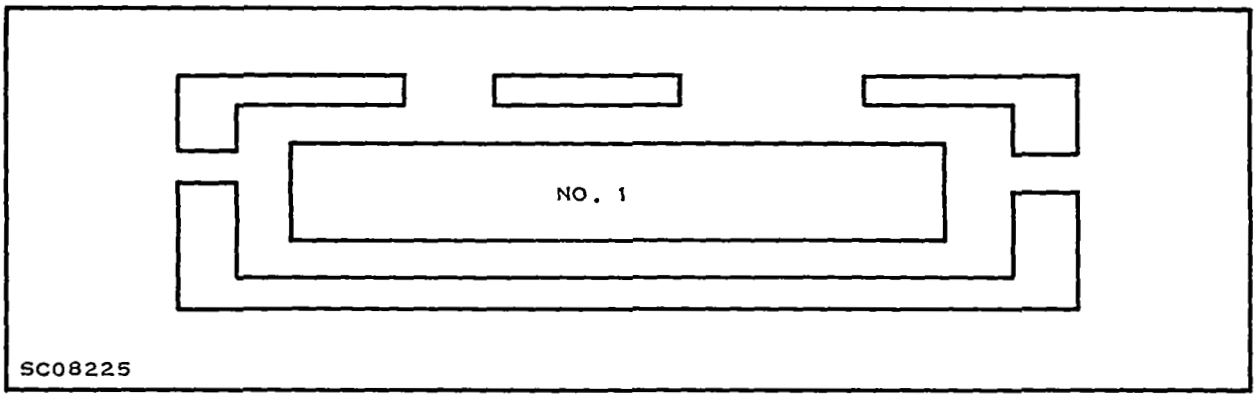


Figure 3-103. Location of Oxide in Window Shown in Previous Figure

The oxide in the windows prevents good electrical connection between the metallization and the silicon of the bar components. Electrical effects of this are an "open" or high resistance in the circuit involved. Methods of discovering this type of condition are curve-tracer tests of the particular circuit where a malfunction or abnormal parameter reading has been obtained. The curve-tracer tests may reveal the high resistance or "open" condition. Sometimes, a corner or portion of the window will be visible before the metallization has been removed. Full evaluation requires the removal of the metallization from the surface of the bar. The methods of removing the metallization are discussed at the beginning of this section (Section IV-C, part 2-e).

The cause of oxide remaining in the windows is usually insufficient etch at the time of window formation. The oxide requires a specific length of time to be etched away by the etch (normally composed partially of hydrofluoric acid). The oxide may be thicker on one portion of the bar than on another, thereby causing most of the bar to have properly formed windows, whereas the thicker oxide portion of the bar would have improperly formed windows. Possibly the etch may have covered one portion of the bar for a longer time than another portion of the bar. This condition normally would exist from the time of manufacture; however, if the condition were marginal, the electrical resistance could increase after manufacture because of oxide dielectric change due to a temperature or voltage variation. The electrical resistance sometimes can be reduced by probe pressure on the window.

c. Open Stitch, Wedge and Ultrasonic Bonds

Stitch and wedge bonds are those usually formed by a combination of heat and pressure between a heated stage and heated capillary. Ultrasonic bonds are formed by the application of ultrasonic energy to the metals being bonded. At the present time the wire used in ultrasonic bonding is usually aluminum whereas stitch and wedge bonds are more likely to occur on gold wire.

Wedge and ultrasonic bonds are used on both ends of the wire connecting the bar to the external terminal. The stitch bond is normally located on the external terminal. The stitch bond is normally located on the external terminal end only. It is normally formed after the ball bond by squeezing the bonding wire between the tip

of the bonder capillary and the external lead with sufficient pressure to form an alloying of the wire to the surface of the external lead. Refer to Figure 3-104 for a cross section of an "open" stitch bond. This particular stitch bond had connected a gold wire to a gold plated kovar external lead.

The electrical effects normally associated with an "open" bond of any kind are an "open" or intermittently "open" external pin. This can be an intermittent condition because of physical contact between the disconnected wire and the bonding pad surface. This condition may not be visible during the initial microscope inspection due to the very small opening which may exist. A threshold test is a method for discovering this condition; however, if the condition is intermittent, the threshold test that is usually performed prior to opening might not reveal the condition. Temperature cycling or vibration of the device either before or after opening the package could be expected to reveal the "open" stitch bond.

The cause of an "open" bond is usually one of the following:

- Improper bonding
- Improper plating of the surface bonded to
- Environmental conditions exceeding design capability of bond.

Improper bonding of a bond can result from too little or too large a pressure by the bonding machine. Incorrect temperature is also a possibility. The surface bonded to must contain adequate and correct material for sufficient alloying to occur.

d. Open Ball Bond

The ball bond is located on the bar-end of the wires connecting the bar to the external terminals. It is normally formed by squeezing the end-of-wire ball between the tip of the bonder capillary and the bonding pad. When the ball and the bond pad are sufficiently heated, alloying of the ball to the bond pad results from squeezing the two together.

An "open" ball bond that occurred because of the formation of intermetallic compounds in a gold-aluminum system is shown in Figure 3-105. The "open" exists at the dark wavy line in the lower portion of the bond.

An open condition in a gold-to-gold system, that resulted from improper bonding conditions, is shown in Figure 3-106. Little or no alloying is visible; this indicates that insufficient temperature or pressure existed during the bonding process. Conceivably, a layer of contamination on the surface of the metallization could also prevent alloying.

A threshold test usually indicates an "open" bond. However, the opens due to intermetallic compound formation frequently are intermittent and easily "snapped in" or closed by application of one volt or more. Great care must be used in analysis of such defects.

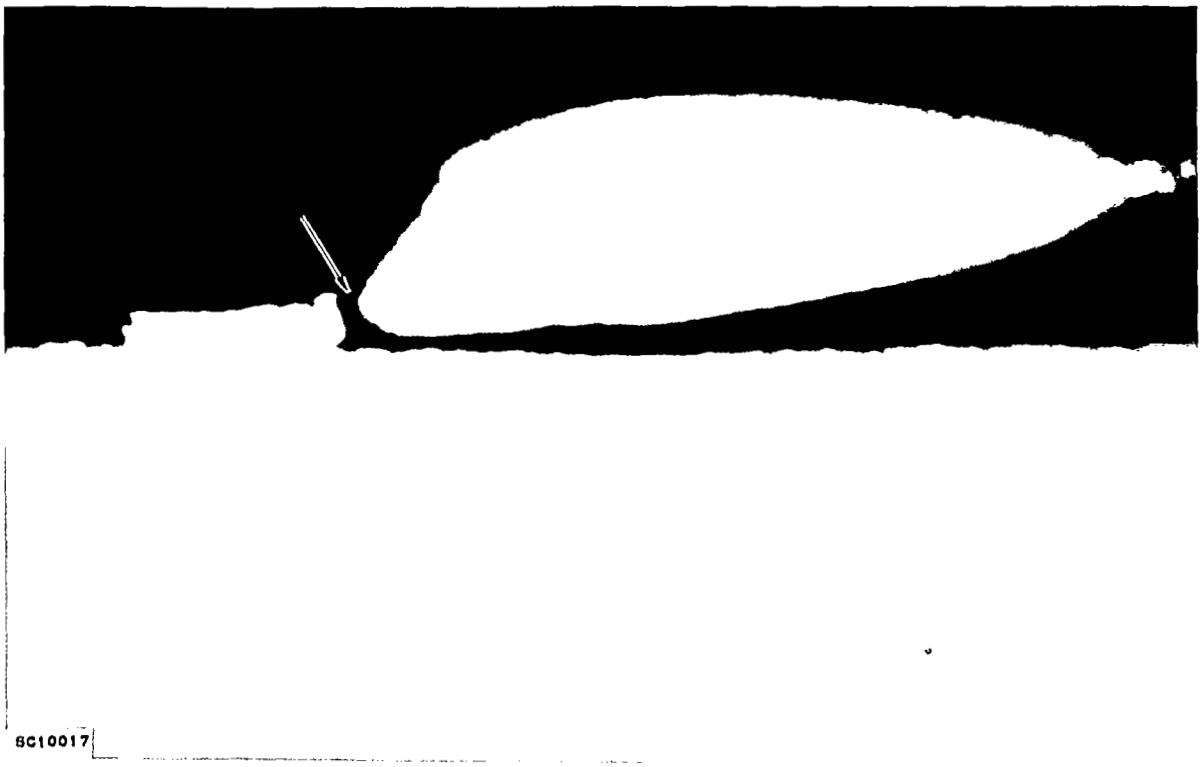


Figure 3-104. Open Stitch Bond

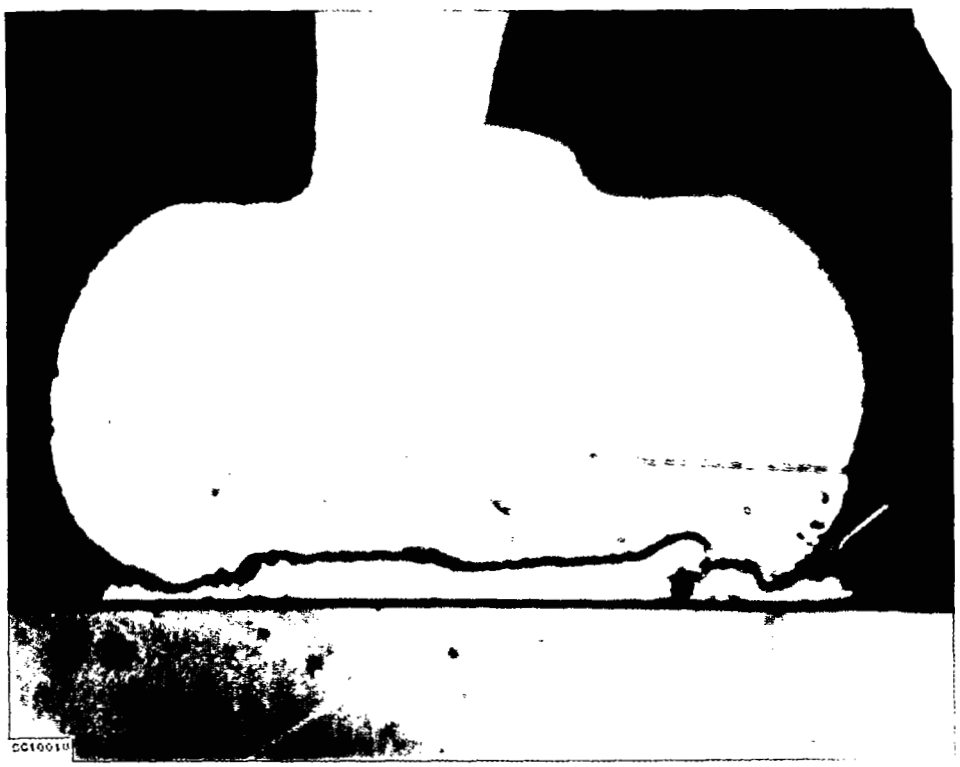


Figure 3-105. Open Ball Bond (Gold-to-Aluminum System)

e. Improper Diffusion

The term "improper diffusion" is defined as the existence of an undesired diffusion at a particular location.

An illustration of an undesired diffusion that connects a resistor to substrate is shown in Figure 3-107. The undesired semicircular bulge on the periphery of the large rectangular area was formed by an incorrect opening in the oxide, which permitted the dopant to diffuse into the silicon. The photograph was obtained by removing part of the silicon dioxide with a planar section, then staining the silicon to bring out the junctions. Additional examples of improper diffusions are shown in Figure 3-108, illustrating two resistors connected by an undesired diffusion, and Figure 3-109, which illustrates an unwanted collector-to-substrate connection.

For the case where a desired diffusion failed to occur, refer to Figure 3-110. The dark collector area has a gap which allows the base to connect to substrate. This probably resulted from incomplete oxide removal prior to collector diffusion.

The electrical effects of improper diffusions vary widely, depending on the location of the defect. Usually a resistive connection exists via the defect between two separate portions of the device circuit. The first step toward locating the affected portions is accomplished by circuit analysis, curve-tracer tests and logic. Frequently a small blemish exists in the oxide above such a diffusion. This may provide a clue to which parts of the circuit are involved. The next step would be to remove a portion of the material by sectioning, and then to stain the silicon.

It is important to differentiate between the linear resistance of an improper diffusion and the nonlinear trace of an inversion (described in succeeding paragraphs). Improper diffusions which do not cause resistive connection between two circuits may cause low breakdown voltage. An example is an emitter diffusion on the edge of a resistor formed during base diffusion: the result is low breakdown voltage at the emitter diffusion, accompanied by light emission. When the breakdown is less than its value under normal circuit operating conditions, improper currents will occur.

f. Oxide Defect (Pinhole)

An oxide defect that was readily visible during initial microscopic examination was discussed and illustrated in a preceding paragraph. Some oxide defects, such as the one shown in Figure 3-111 are small and hidden under metallization. The defect is the small circular area with a white center. A small hole (commonly called a pinhole) in the oxide permitted any metallization which may have been deposited over it to make electrical contact with the underlying silicon.

SC10019

Figure 3-106. Open Ball Bond (Gold-to-Gold System)

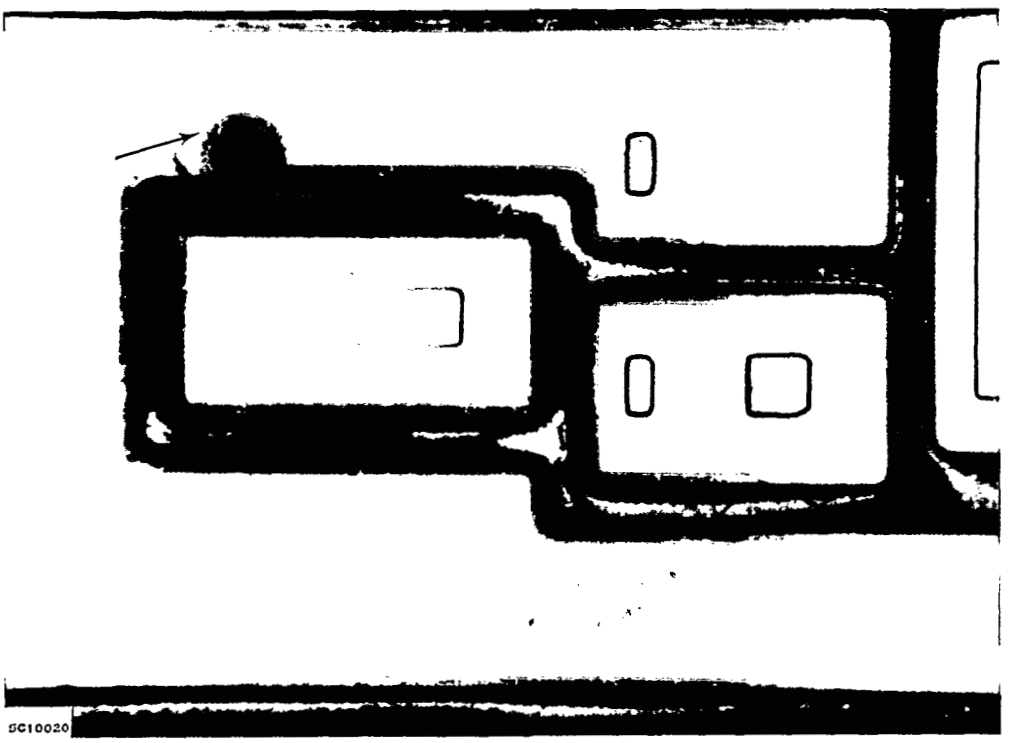


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Figure 3-107. Resistor-to-Substrate Short Due to Improper Diffusion

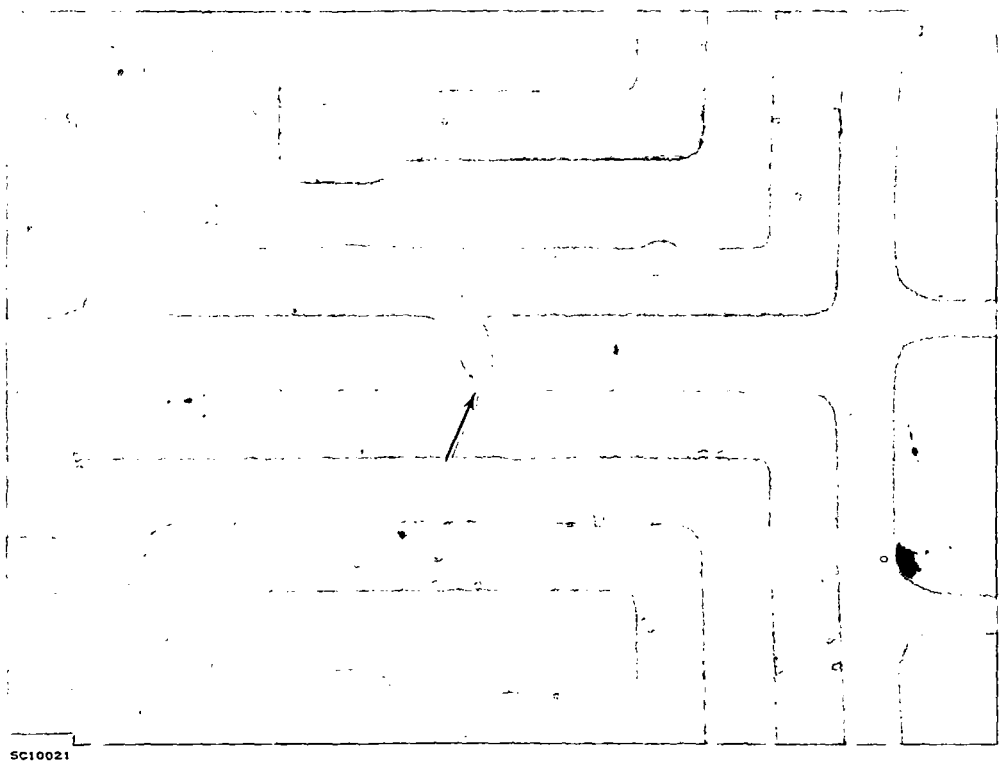

Figure 3-108. Resistor-to-Resistor Short Due to Improper Diffusion

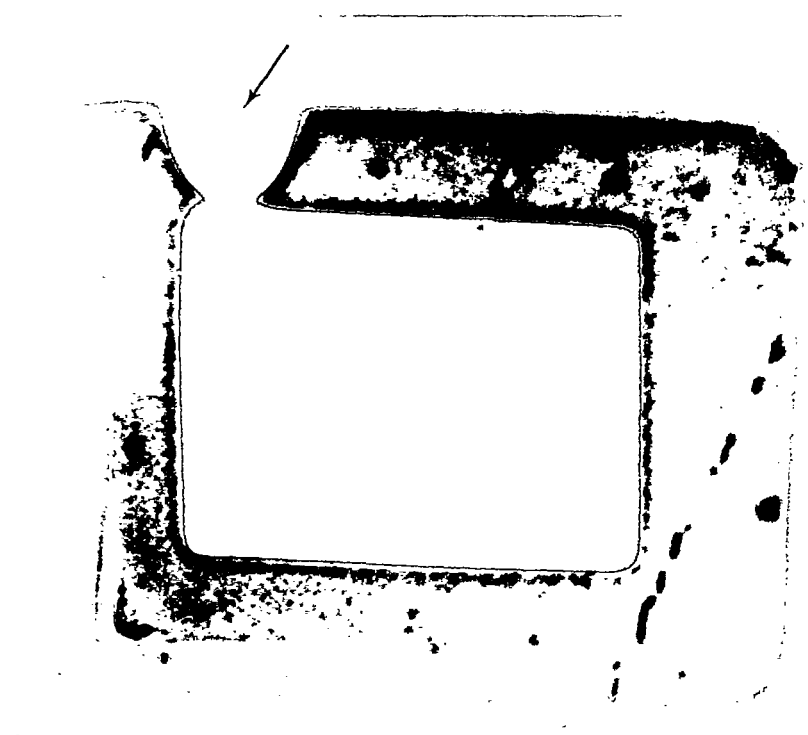

Figure 3-109. Collector-to-Substrate Short Due to Improper Diffusion

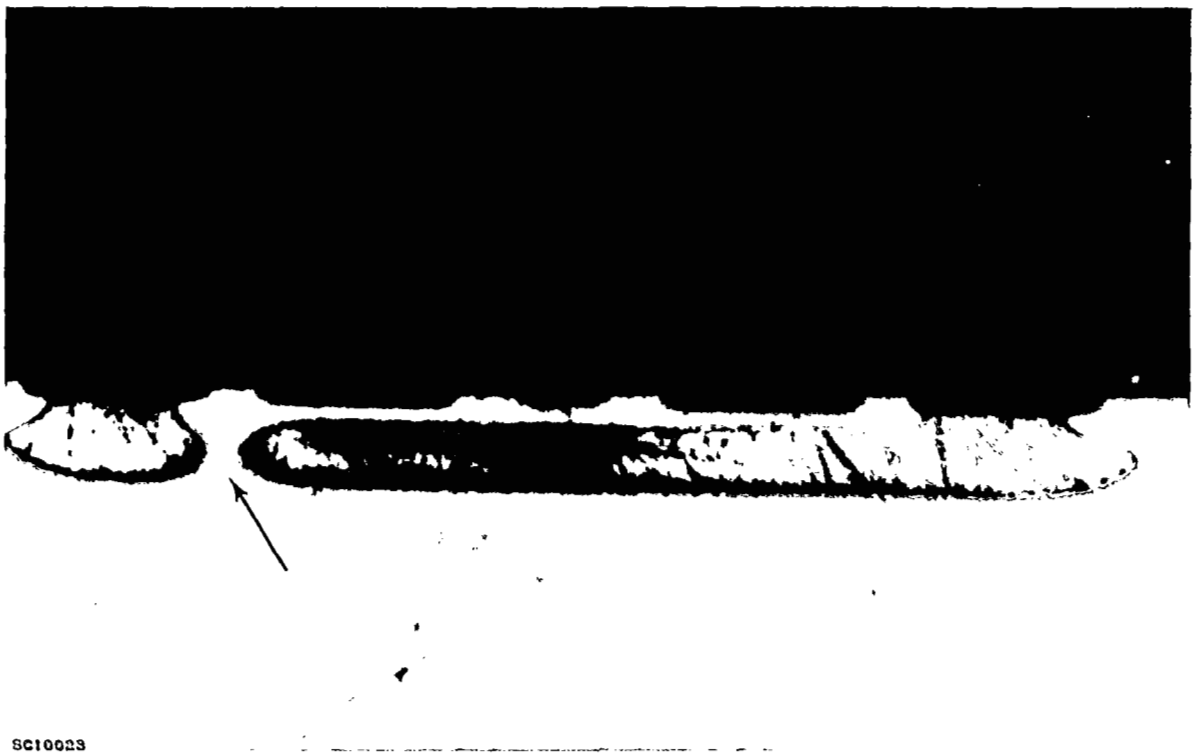

Figure 3-110. Base-to-Substrate Short Due to Improper Diffusion

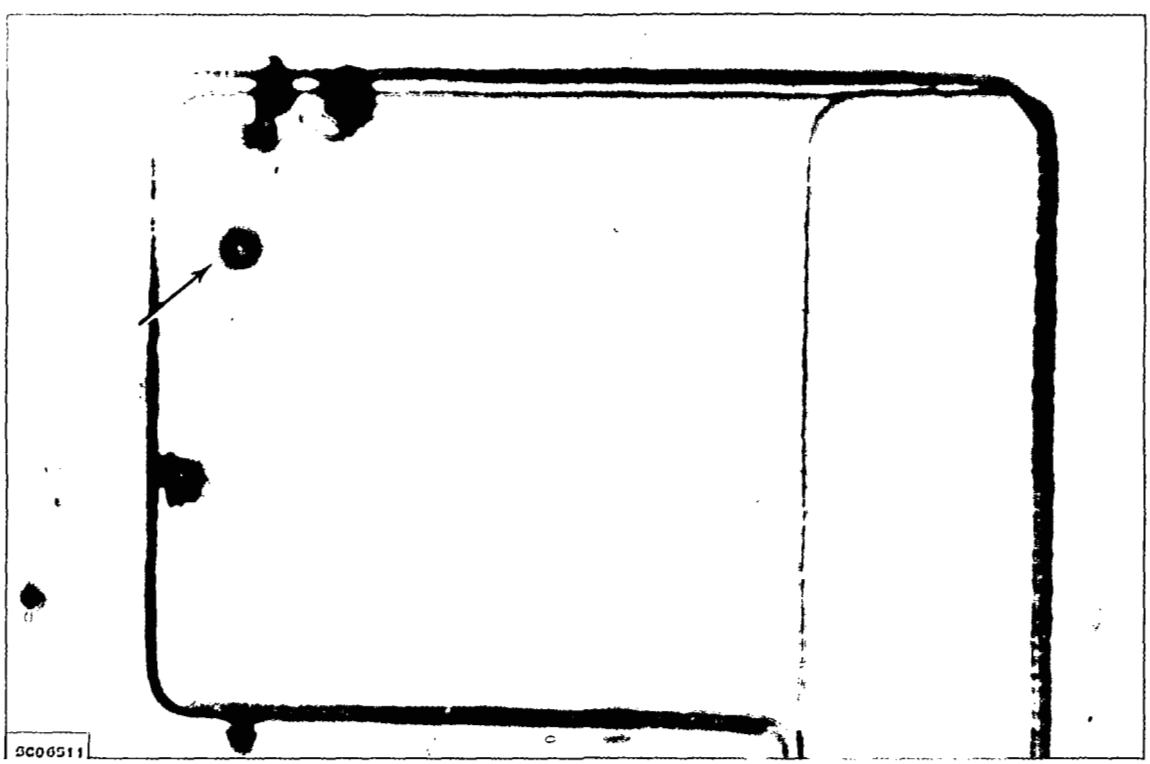

Figure 3-111. Oxide Pinhole after Removal of Metallization

The electrical effects of an oxide defect depend upon the portions of the circuit which are connected together. Curve-tracer measurements of this type of defect usually show a linear resistive connection. Occasionally, a diode indication is encountered. This is thought to result from either a point-contact phenomena or an actual diode produced by diffusion into the pinhole area.

g. Inversion

"Inversion" or "channeling" failures are sometimes encountered following burn-in or elevated temperature tests. Transistors, and infrequently resistors, are found to be degraded by this type of defect. Two of the more common situations involving transistors are inversion of the base of an NPN, and inversion of the collector of a PNP.

An NPN base inversion often has the appearance shown in Figure 3-112, when measuring from emitter to collector with a curve tracer. A change of polarity may alter the current level but not the basic shape of the curve. Emitter-base and collector-base breakdowns remain normal, with no leakage apparent.

A collector inversion of a PNP transistor appears essentially the same as the NPN case when measuring from base to collector with a curve tracer. The junction must be reverse biased. The base-emitter breakdown remains normal. The emitter-collector characteristic appears as in Figure 3-113.

Inversions such as those, discussed here will disappear when the device is heated to 200°C for several hours. Behavior of this nature is typical of abnormal ionic surface states.

Electrical effects resulting from inversions depend largely on the circuitry involved. An inverted transistor exhibits high-leakage currents and a lower than normal V_{off}. These abnormal transistor characteristics are readily observed if the transistor is accessible at the external pins of the monolithic microcircuit. Otherwise, probing is necessary to locate such a condition.

More information concerning inversion phenomena may be found in a continuing series of volumes entitled "Physics of Failure in Electronics" issued by Rome Air Development Center and Battelle Memorial Institute, Volume 5. The latest of the series was published in June, 1967.

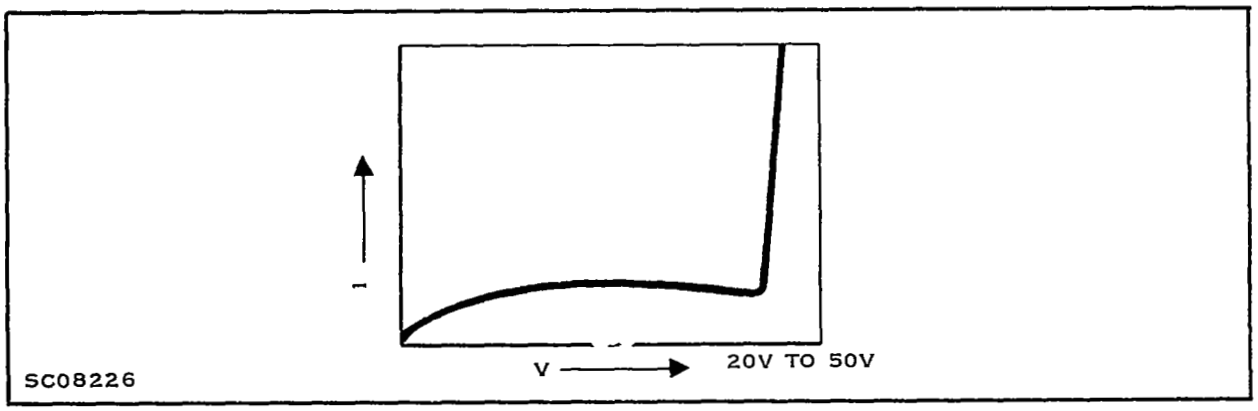

Figure 3-112. NPN Base Inversion C-E Test;
PNP Collector Inversion B-C Test

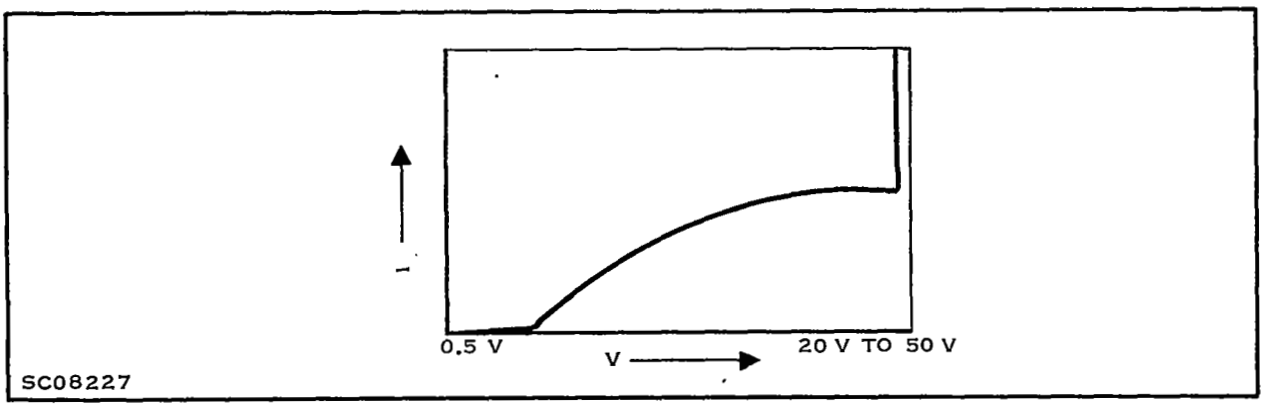

Figure 3-113. PNP Collector Inversion C-E Test

D. REFERENCES

1. Richard B. Hurley, Junction Transistor Electronics (New York: John Wiley and Sons, Inc., 1960), p. 431-2.

2. Loc. cit., Richard B. Hurley, p. 27.

3. Op. cit., Richard B. Hurley, p. 431-2.

4. Chih-Tang Sah, "Effect of Surface Recombination and Channel on P-N Junction and Transistor Characteristics," IRE Transactions on Electron Devices, Vol. ED-9 (January 1962) pp. 94-108.

5. Motorola Inc., Quarterly Report No. 3, Detailed Study of Deleterious Effects on Silicon Transistors, dated December 1964, Contract No. AF 30(602)-3044, p. 39.

SECTION V

METALLURGICAL SECTIONING OF THE SEMICONDUCTOR ELEMENT

A. GENERAL

Metallurgical sectioning is the term used to describe the procedure for obtaining a cross section of a metallurgical sample. A cross section enables one to examine the internal physical or chemical characteristics of the sample. Generally, this is utilized to relate the present condition of the sample to a failure mechanism or mode. However, it is useful for other purposes such as determination of plating thickness, junction depths, or chemical composition.

The procedural steps for sectioning are:

- Encapsulation
- Coarse grinding
- Fine grinding
- Rough and fine polishing
- Staining, if necessary

Encapsulation requires that the entire sample be held securely to maintain the original orientation of the separate parts. Any movement might prevent an effective analysis of the failed part. Grinding and polishing make necessary the removal of nonessential parts of the sample, and the exposure of the area to be studied. Staining is sometimes necessary to reveal detail otherwise not visible, and for the removal of surface damage.

B. ENCAPSULATION MATERIAL AND TECHNIQUES

1. Encapsulation Material

The encapsulating material should be selected with consideration for the following properties:

- Hardness. Usually, a hard material is necessary to prevent excessive "rounding" at the sample-plastic interface.
- Transparency. Transparency is desired to allow observation of the sectioning progress in relation to the surface geometry.

- Shrinkage. This should be low to prevent compressive and/or tensile stresses on the sample.
- Adhesion. A high degree of adhesion between sample and the encapsulant is absolutely necessary.
- Mounting Pressure. None. Little or no pressure is desired, to prevent damage to delicate structures.
- Curing Temperature. The curing temperature should be low to prevent damage to the sample; usually, less than 100°C is desirable. When encapsulants such as epoxy are used, the internal temperature of the sample will rise because of the heat generated by curing. This internal heat rise can be minimized by the optimum selection of resin-catalyst ratio, minimum encapsulant volume and lower curing temperatures.
- Viscosity. The viscosity should be low to allow complete immersion of the sample, i.e., no bubbles at the various epoxy-sample interfaces.

2. Encapsulation Techniques

a. Surface Cleanliness

After the device has been properly opened, examined and photographed, it is prepared for mounting. A major concern is the surface cleanliness of the device. All foreign material must be removed from the surface of the device before encapsulation, otherwise, poor adhesion and poor sectioning results may be expected. All surface protectants, if any, such as varnish, silicones, etc., must be completely removed before encapsulation. There are many different techniques for removing surface protectants and cleaning the surface of the device, but it must be remembered that whatever process is used, it must result in little or no damage to the surface of the device. Unless time is critical, a slower cleaning procedure is usually more satisfactory.

b. Specimen Holder

The second consideration in encapsulation is the specimen holder. The holder must orient the device in the proper plane for sectioning, be transparent enough to allow observation of the sectioning progress, be large enough for the operator to control the various sectioning steps easily, and be compatible with the encapsulating material. Ordinarily, this function is best served by a cylinder of plastic material, Figure 3-114. These holders may be made from plastic rod stock by using standard machining procedures or by making a simple silicone rubber mold from an original part and then casting additional holders from the same epoxy used for encapsulation. This latter procedure also results in a completely compatible system of encapsulation, with uniform properties throughout the sample.

Figure 3-114 Plastic Holder

c. Epoxy Encapsulant

Another step that must be done with precision is the measuring and mixing of the resin and catalyst forming the epoxy encapsulant. Since the ratio of catalyst to resin is critical for this application, it is recommended that a burette system be employed for the accurate dispensing of both ingredients, as shown in Figure 3-115. The catalyst-to-rewin ratio suggested by the manufacturer should be initially used until repeatable results with the system are obtained. If the desired properties are not obtained, then the ratio may be varied until these properties are generated. Generally, increasing the amount of catalyst in the mixture will cause the epoxy to be harder, will increase shrinkage, and augment the exothermic reaction during curing. The best mixing vessel is a polyethylene beaker of 25-to-50 ml volume. If the beakers are cleaned after use, they may be reused many times. It is most advantageous to begin gentle stirring immediately after the resin has been added to the catalyst, in order to minimize the formation of bubbles. Two-to-five minutes of continuous agitation is sufficient to thoroughly mix the ingredients. Examination of the mixture should reveal a completely homogenous solution without any apparent separation of the ingredients. Care should be exercised to keep the catalyst out of contact with the stock of resin. To keep the possibility of contamination at a minimum, it is best to use a disposable stirring rod.

d. Evacuation of Air from Surface of Device

An important aspect of sample preparation is the evacuation of the air naturally entrapped on the surface of the device. If this is not done properly, voids will appear in the hardened section that will allow the sample to shatter or fracture. For this purpose, a simple vacuum system with a roughing pump capable of evacuating a 3-in bell jar is all that is necessary (Figure 3-116. This can best be done by placing the mixed epoxy solution in its container in the bell jar; then the vacuum should be gradually increased until full outgassing of the epoxy mixture is obtained. The most desirable means of controling the vacuum is a manually operated valve. If a full vacuum is pulled immediately, the mixture will boil violently and expel the contents of the beaker onto the interior of the bell jar. However, even slow evacuation of a 25-ml mixture of epoxy should not take more than a few minutes. Depending on the epoxy used, longer pumping times may allow initiation of the epoxy curing process, which is definitely undesirable. When bubbles are no longer released from the epoxy, it may be poured over the specimen in its holder. With the sample immersed in the evacuated, uncured epoxy in its holder, it is placed back into the vacuum system. The sample is then pumped until only a few bubbles are released. This second evacuation is absolutely necessary to remove the air entrapped within the sample and the air taken in submerging the sample. This will insure adhesion of the epoxy to the sample and its holder without an interfering film of air at the interfaces. Also, all of the cavities and structure will then be fully supported by the encapsulant. Curing of the epoxy is done by following the recommendations of the manufacturer. To adequately cure most epoxies, all that is needed is a small specimen

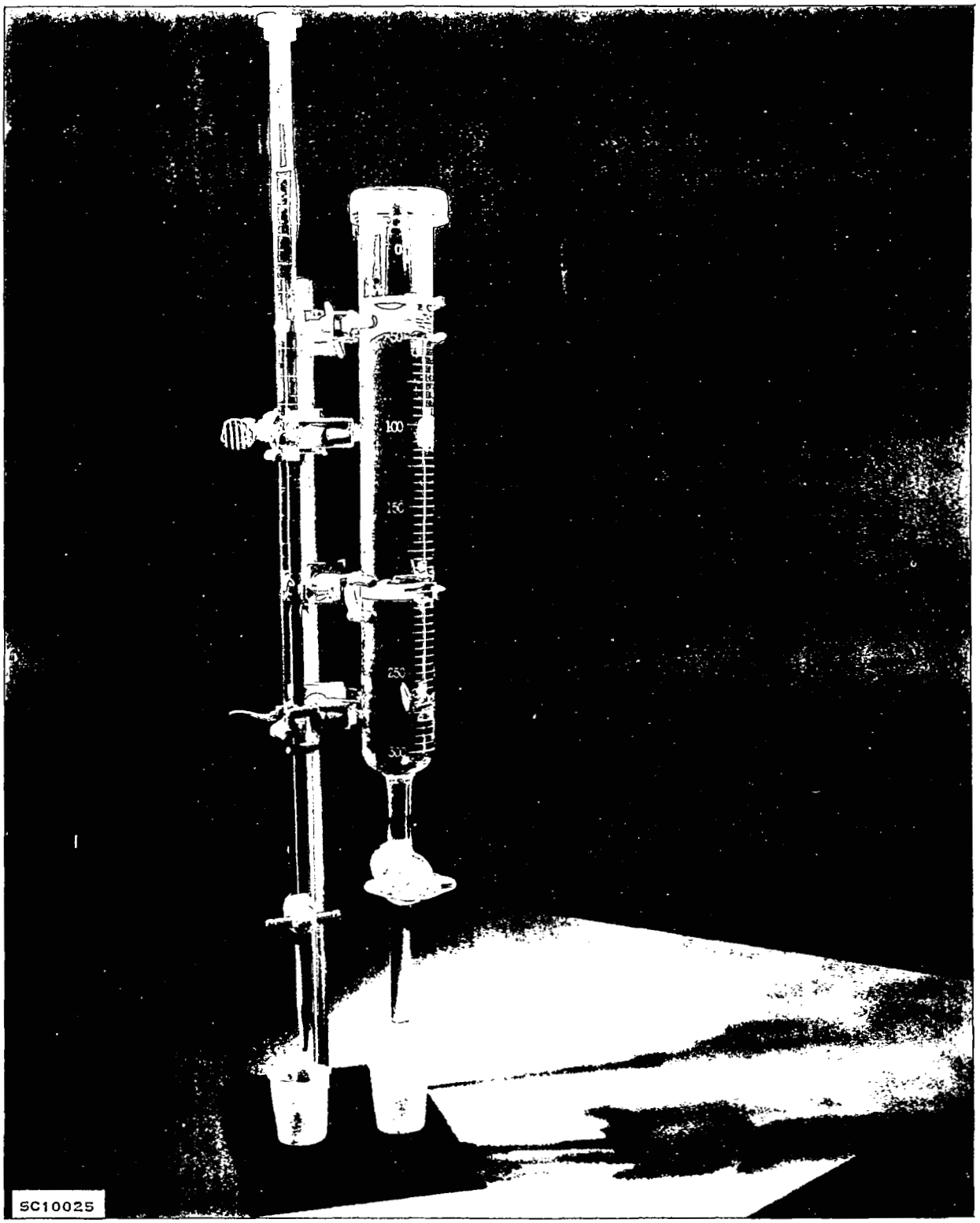

Figure 3-115. Burette System for Dispensing Epoxide and Catalyst

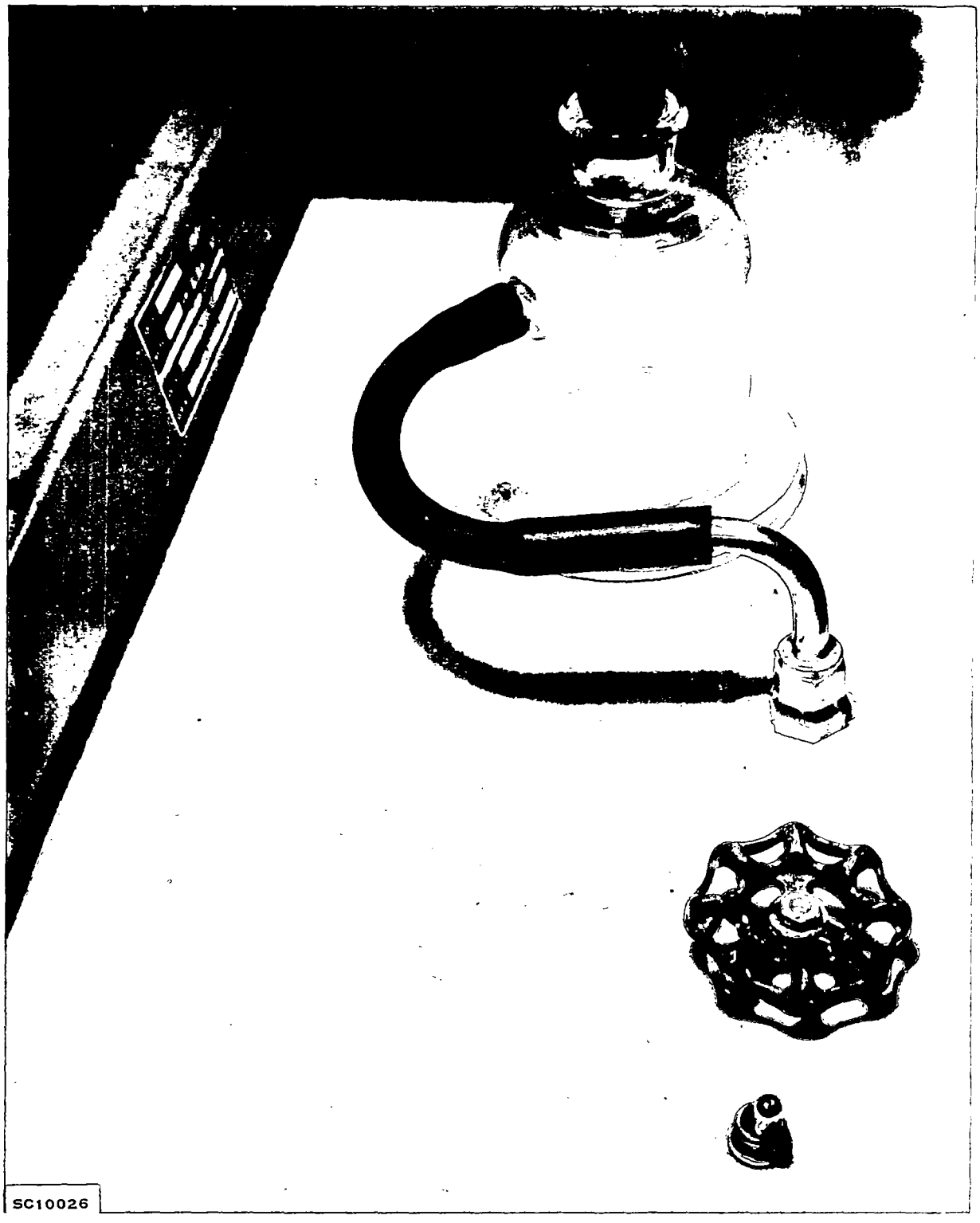

Figure 3-116. Vacuum System for Outgassing Epoxy Mixture

oven with a good thermostatic control. After the encapsulant material has been thoroughly cured, the specimen is ready for the next operation, coarse grinding.

C. COARSE-GRINDING EQUIPMENT AND TECHNIQUES

The purpose of coarse grinding by means of a metallurgical-belt surfacer is solely to remove excess material and achieve a rough orientation on the area of interest in the sample. Belts are available with grit numbers of either 80, 120, 240, 320, 400 or 600. The relationship between grit number and median abrasive particle size (measured in micrometers) is shown in Figure 3-117. Experience indicates that coarse-grinding the sample is most efficiently done by the use of a metallurgical belt surfacer using 120-mesh grit, silicon carbide abrasive belts and water as an effluent. The sample is held firmly in the hand in the proper orientation for the sample in question (Figure 3-118). It is then placed in firm, complete contact with the moving surface. The rate of water flow should be sufficient to keep the belt surface free of the material being removed but not great enough to cause splattering over the work area.

NOTE

> The belt should never be allowed to come into contact with the chip, since this will result in gouging and shattering the chip, which may be impossible to correct later.

Care should be exercised to maintain the orientation of the section, otherwise "rocking" of the sample will result in faceting of the plane surface. Faceting will make it difficult for the analyst to locate and polish the area of interest. It is desirable to grind down to within 0.010 inch of the sample if this can be done without contacting the chip or assuming some other unnecessary risk.

D. FINE-GRINDING EQUIPMENT AND TECHNIQUES

The purpose of fine-grinding is to remove the damaged zone produced by the coarse-grinding operation. (A high-torque, low-speed metallurgical fine grinder (163 rpm/246 rpm) is recommended for this task). However, while the damage produced by coarse-grinding is being removed, another layer of less extensive damage is being formed by the finer abrasive grains of the fine-grinding cycle. The damage resulting from the fine-grinding operation is not as severe nor as deep as the first-layer (coarse-grind) damage. As the fine-grinding operation continues, progressively finer abrasives are used. Each succeeding layer of damage is lessened until, finally, the remaining deformation can be removed by rough polishing.

The record of experience in a failure analysis laboratory has proven that silicon carbide abrasive papers are best for fine-grinding. Resin-bonded material should be utilized because it can be used with a lubricant, flowing water, thereby preventing overheating of the sample and carrying away the debris resulting from fine grinding.

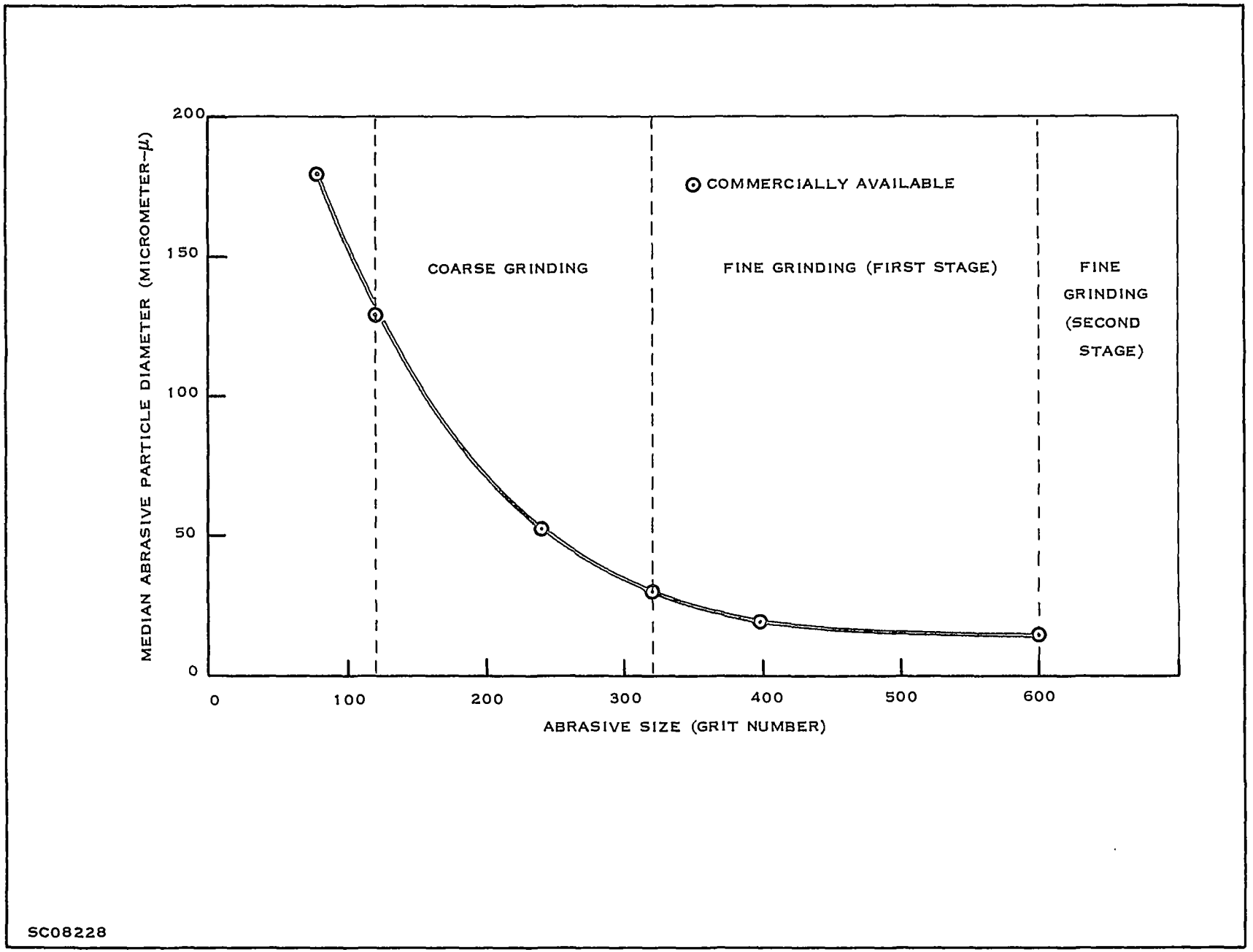

Figure 3-117. Abrasive Size Range for Grinding

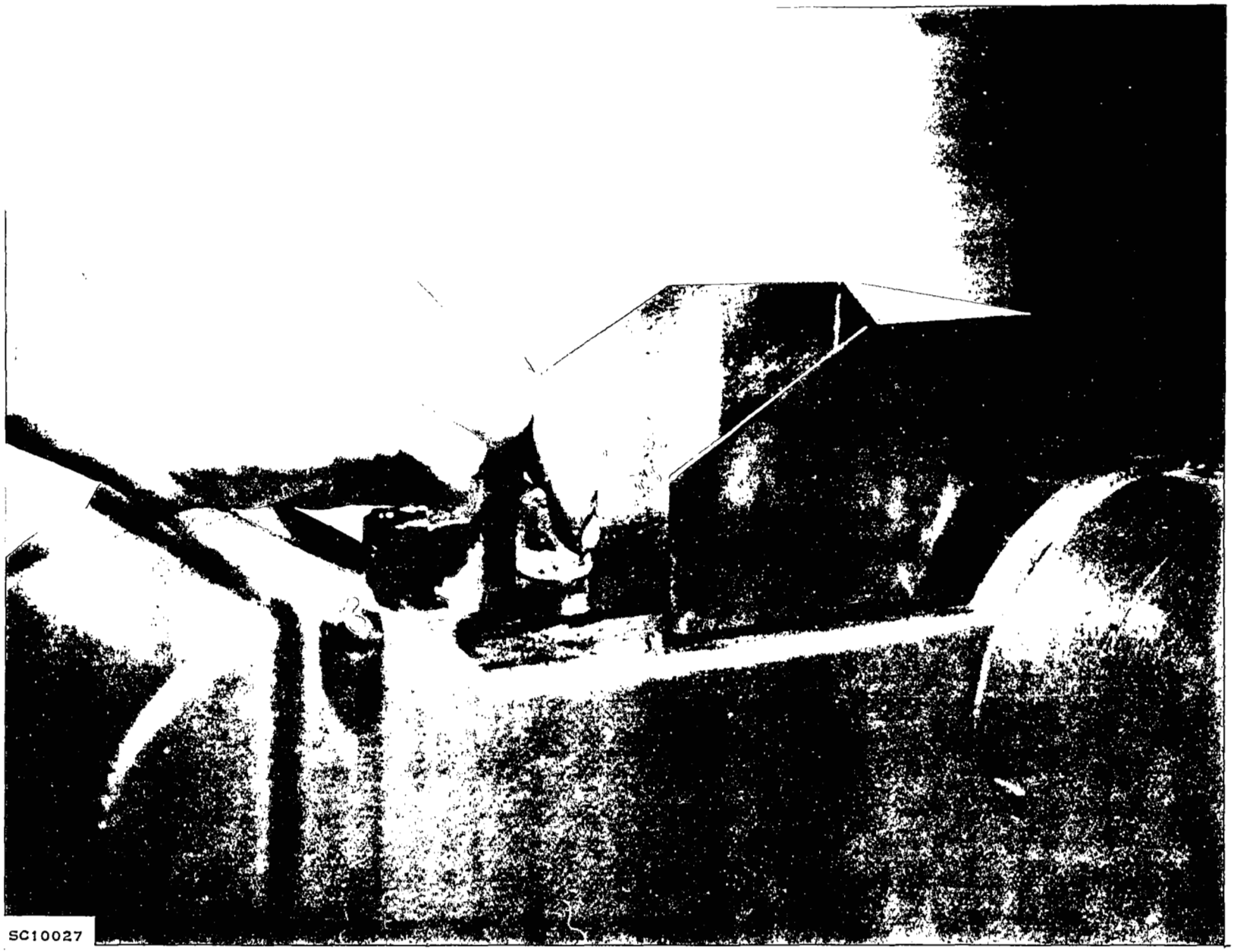

Figure 3-118. Sample Holder Properly Oriented on Belt Surfacer

For the fine-grinding operation, the alignment of the face of the plane being ground is made with respect to the pertinent geometry of the specimen. If the specimen has been properly encapsulated, contact of the silicon wafer with the wetted paper will not cause severe damage to the wafer. For most devices, it is safe to grind to within 0.002 inch of the desired location, using 320-grit silicon carbide paper. The final fine-grinding operation can best be done using fresh 600-grit paper. This step will remove material down to the very edge of the region to be examined. With running water as a lubricant, the sample should be held in even contact with the rotating wheel (Figure 3-119). The sample should be frequently examined to determine progress and maintain proper orientation. Careful observation of the abrasive surface of the wheel should be maintained during this final (most-fine) fine-grinding operation. Even with water as a lubricant, the fine abrasive surface will gradually clog with removed-surface debris. When this occurs, gouging and burnishing of the sample surface will result. For this reason, the 600-grit paper should be frequently replaced. It should be remembered that the damage from a scratch may extend from ten to as much as fifty times the depth produced by the abrasive grain. The average scratch depth produced during coarse- and fine-grinding operations is shown in Figure 3-120.1/

E. ROUGH-POLISHING EQUIPMENT AND TECHNIQUES

The results achieved in the final polishing operation are to a large extent determined by the techniques employed during the rough polishing step. A medium/high-speed rough polisher (550 rpm/1150 rpm) is satisfactory for this operation.

Ideally, the rate of removal during polishing should follow a gradual, linear decrease. The best abrasives to be used to approximate this curve are the oil-soluble diamond abrasive pastes. A well-graded (extra fine) abrasive is more effective when the polishing film is thin. Therefore, oil is a better lubricant because the adhesive force between the sample surface and the polishing cloth is greater, which means that the polishing film is thinner. It is normal to expect a sharp drop-off in the rate of removal when abrasives other than diamond are used for the rough-polishing operation, as noted in Figure 3-121.1/

Diamond abrasives are well suited for rough polishing because of the constant high cutting-rate achieved by the use of the relatively fine 4-to-10 μm particle size. This is caused by the tendency of the diamond particles to cut the material rather than to flow over it. The resulting surface has a high luster with few scratches. Abrasives other than diamond are frequently used, but the particle size has to be much larger to produce an equivalent removal rate and, of course, the damaged layer will be much deeper.

Enough time must be spent on the rough polishing operation to remove all of the abrasive deformation. Diamond abrasives have only one criteria for use, a heavy hand. This will achieve the high removal rate desired in this operation. In order to reduce relief or "rounding" of the sample, it is important to use a cover (a napless cloth such as nylon) on the rotating wheel. The initial charging of the wheel is accomplished by

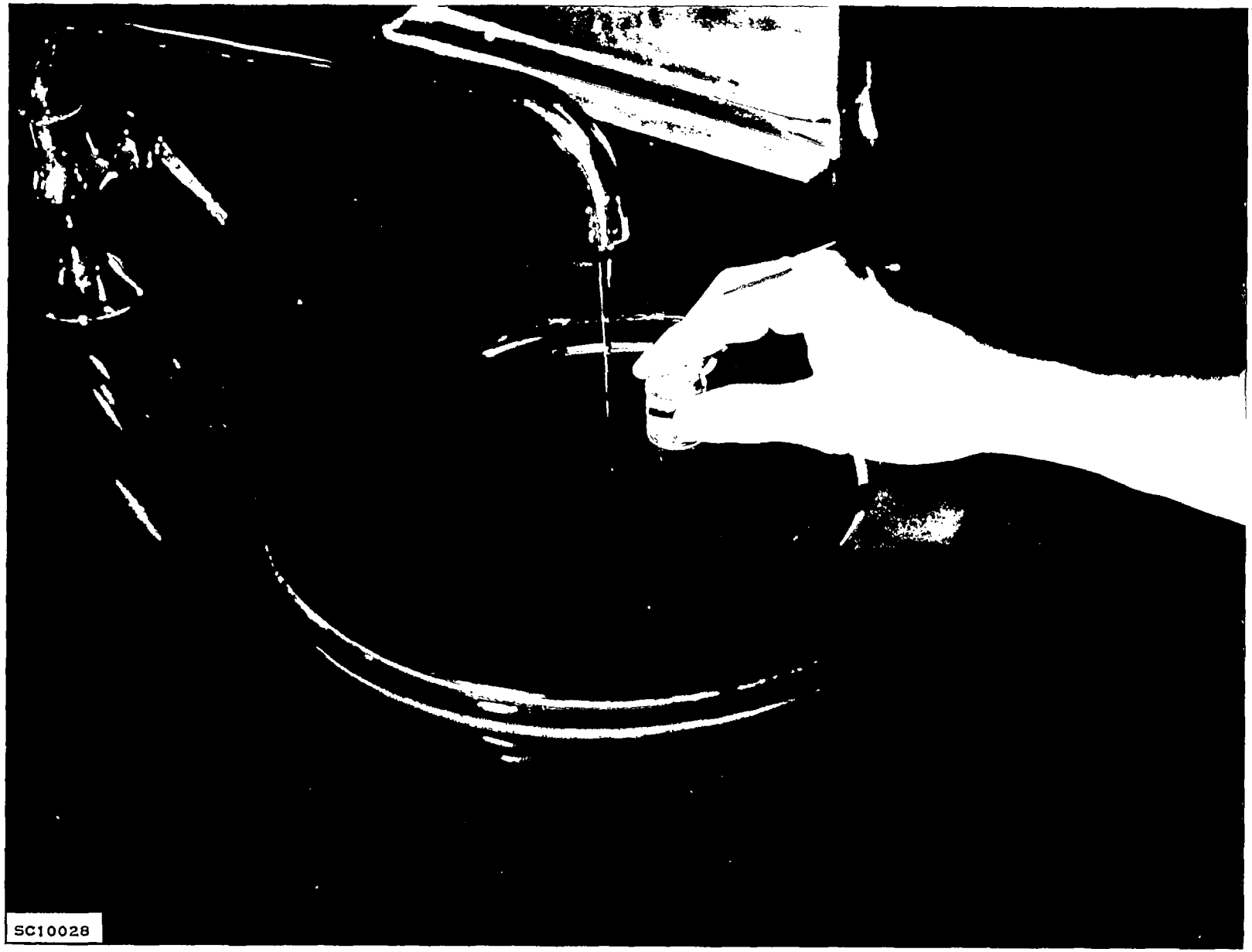

Figure 3-119. Sample Holder Properly Oriented on Fine Grinder

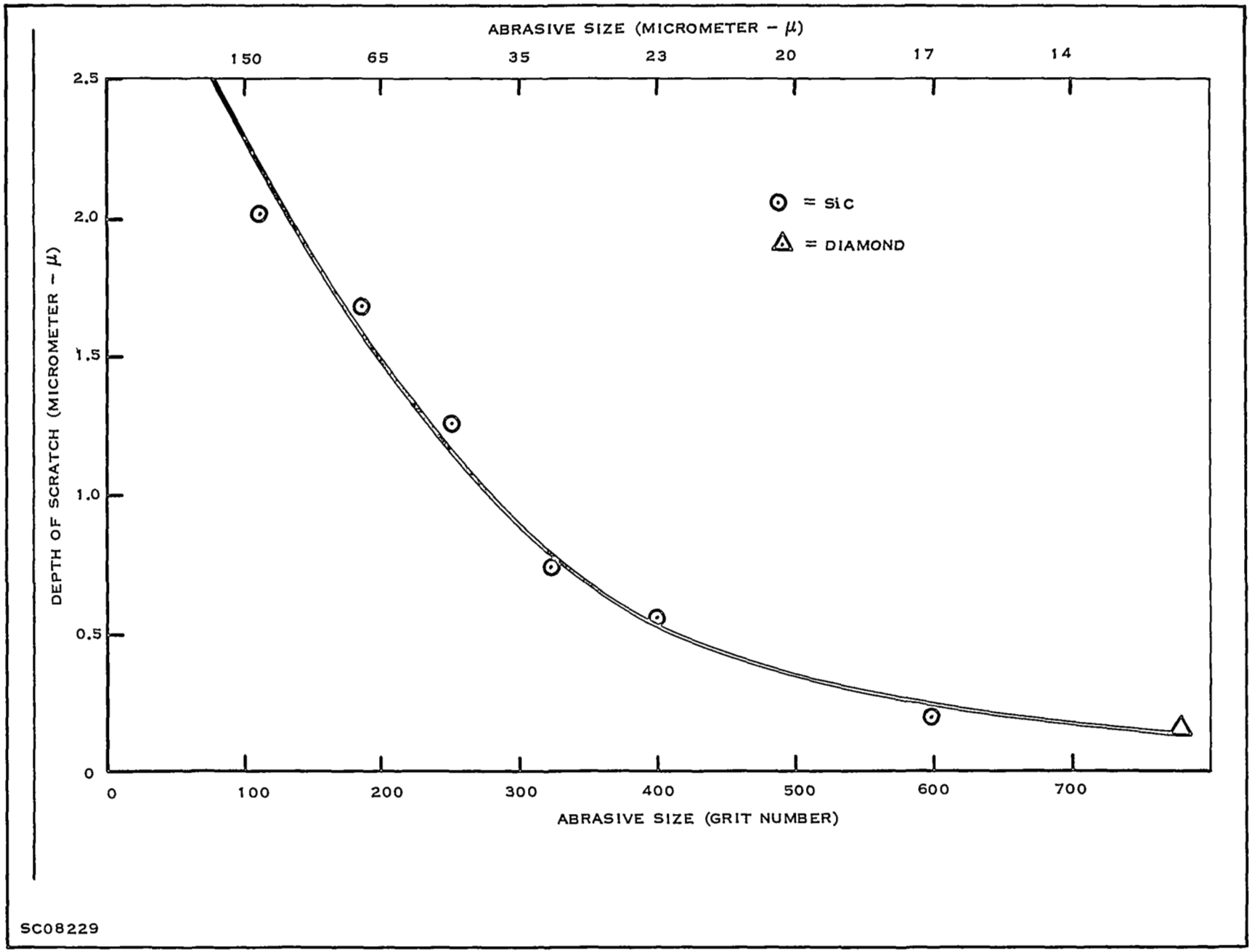

Figure 3-120. Average Scratch Depth (Depth of Scratch versus Abrasive Size)

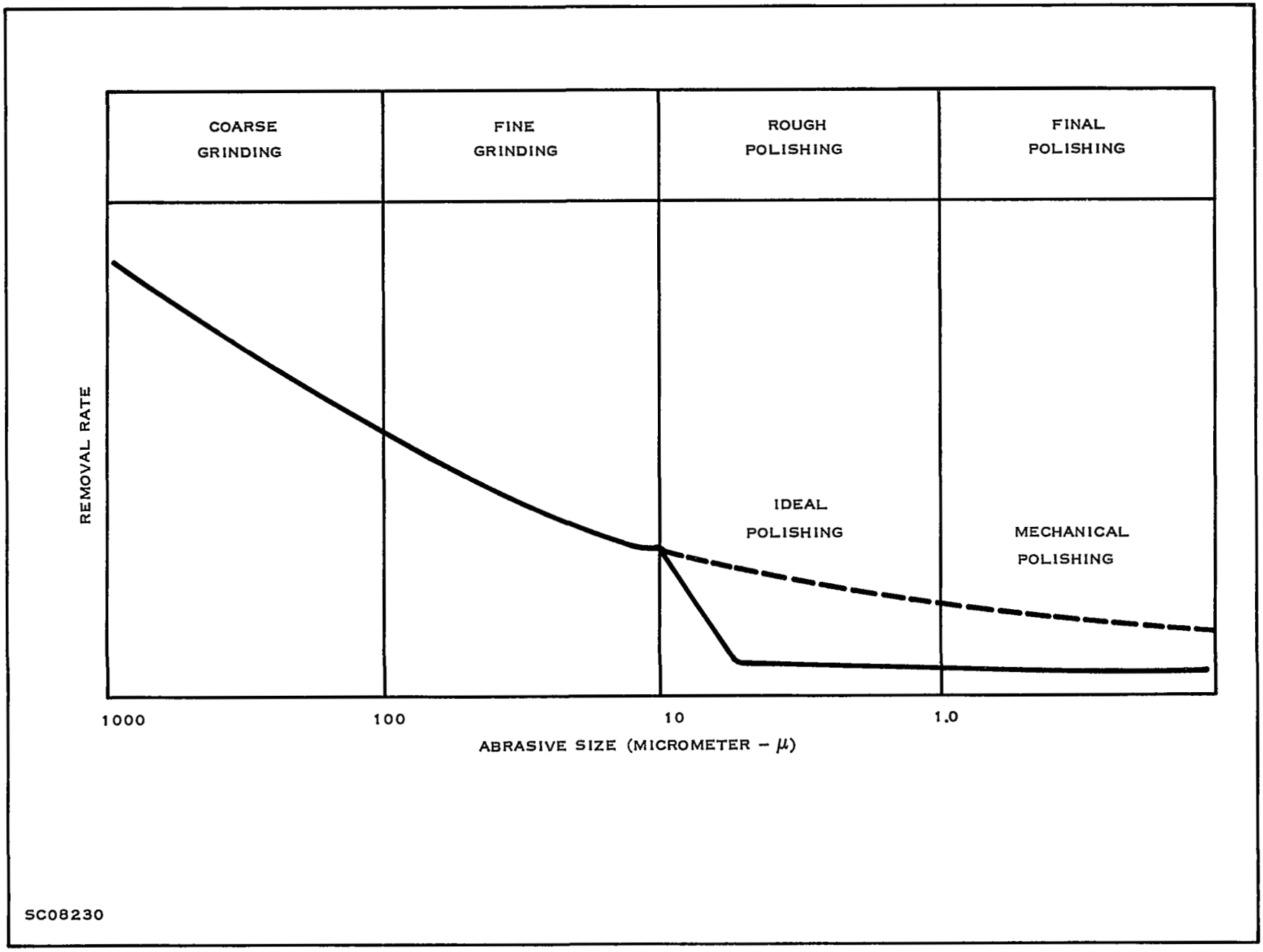

Figure 3-121. Rate of Removal of Excess Material from Sample During Rough Polishing (Rate of Removal versus Abrasive Size)

applying a one-quarter to three-quarter inch ribbon of diamond paste to the surface of the wheel. This can be spread over the wheel by daubing with a clean fingertip. Care must be taken to see that the cloth used on the wheel is taut during the operation to prevent undercutting or "rounding" of the sample. The sample should be carefully cleaned after each step of progressively finer diamond paste, to prevent contamination of the finer abrasive wheels by the coarser particles. Longer times should be spent with the coarser diamond pastes, followed by progressively less time on each succeeding finer abrasive. This is done to reduce the relief effects. The final abrasive in the rough polishing operation should be chosen on the basis of the first abrasive to be used in the final polishing procedure. After completing the application of this final abrasive, damaged layers will be present just as in the cross section of the specimen after the fine-grinding operation, but to a lesser degree.

F. FINE-POLISHING EQUIPMENT AND TECHNIQUES

The next operation in metallurgical sectioning of the semiconductor element is the final or fine-polishing operation. If this final polishing operation is properly completed, and if it is assumed that the rough-polishing operation was correctly done, the true microstructure will be present on the surface of the sample. If an insufficient amount of the surface has been removed, scratches will probably be evident. If any metals are present in the silicon cross section, then metal-flowing may cover the scratch, which may not become visible until after staining. These anomalies will be present to an even greater degree if any of the preceding operations were not properly performed. If any traces of the outlined anomalies are observed after staining, repeating the final polishing operation will usually remove them.

From the many available abrasives for final polishing, two are most suitable for this step—chromium oxide and aluminum oxide. The aluminum oxide is available in several forms, the most useful of which is the 5-μm levigated form, the 1.0-μm and 0.5-μm sizes in the alpha form, and the gamma form in the 0.05-μm size. The alpha form has a hexagonal lattice structure, while the gamma form is cubic in nature. The hardness of the alumina lies just above 9 on the Moh scale, with the alpha type being slightly harder than the gamma type. Chromium oxide is about 15 μm in particle size and is frequently used as the initial polishing abrasive. A medium/high-speed fine polisher (550 rpm/1150 rpm) should be used for this polishing operation.

At this point, it is well to point out a few guide lines concerning cleanliness. Caution must be exercised to prevent contamination of a finer grit operation with a coarser grit from a preceding operation. When proceeding from a coarser grit operation to a finer one, the sample must be thoroughly washed in filtered, deionized water, dried and examined for contamination. The sample should not proceed to the next operation without being completely free of foreign material.

Since napped cloths are most often used for final polishing, it is advisable to keep polishing times at a minimum. The compressibility of the nap allows conformation to the surface of the specimen, resulting in "rounding" of the specimen. This is to be expected, since the softer materials are polished away more rapidly than the harder materials. If sufficient relief is produced in the specimen, the depth of field in the microscope at high magnifications might be too shallow to provide adequate sharpness. Also, the distortion of the interfaces caused by the anomalous reflections can easily introduce serious interpretive errors.

The mounting of the polishing cloth to the wheel and the subsequent preparation of the wheel are both very important. The cloth material, such as microcloth, should be tightly stretched to prevent wrinkling and "pile up" in front of the sample during polishing. To prevent stretching of the cloth after mounting, soak the cloth in water for a time before mounting to the wheel. After mounting the cloth, it should be charged with the appropriate polishing compound. Most of the alumina polishing compounds can be purchased with the abrasive already mixed into an aqueous suspension ready for use. However, chromium oxide, a dry powder, must be mixed with water prior to use. The optimum mixture, determined by experience, is 40 ml of the dry powder to 200 ml of filtered, distilled water. The powder and water mixture should be thoroughly agitated before being applied to the wheel. A good applicator is a polyethylene washing bottle. The wheel should first be wetted with deionized or filtered water before applying the polishing mixture. Set the polisher wheel into rotation at the appropriate speed and apply the mixture to the center of the wheel. Allow the cloth to be completely colored with the polishing compound before proceeding. Care should be used to avoid overcharging the wheel, because this does not improve the polish or the rate of removal and is unnecessarily messy. A good method for preventing overcharging is: after charging, stop the wheel and flush the cloth surface gently with water until the waste water is clear. The wheel is now ready for use. During its use, an occasional 4-ml to 5-ml application of the polishing mixture, followed by 4-to-5 ml of deionized or filtered water, will serve to keep the wheel charged and wet. A properly charged wheel should leave a hazy film on the surface of the specimen after a 5- to 10-second drying time.

As in the earlier operations, particular care should be exercised in holding the sample correctly in order that rocking due to the friction between it and the wheel is minimized. Since most wheels rotate in a counterclockwise direction, the sample should be moved around the wheel surface in a clockwise direction. This polishes the surface from all directions and diminishes smearing, preferential polishing and rounding of the sample. In this manner, as illustrated in Figure 3-122, the sample is rotated around the wheel with sufficient hand pressure to keep in contact with the cloth. In the first stage of polishing, 3-to-4 pounds of hand pressure at a wheel speed of 550 rpm will produce rapid polishing. Two-to-four minutes of polishing under these conditions will normally result in a relatively smooth surface.

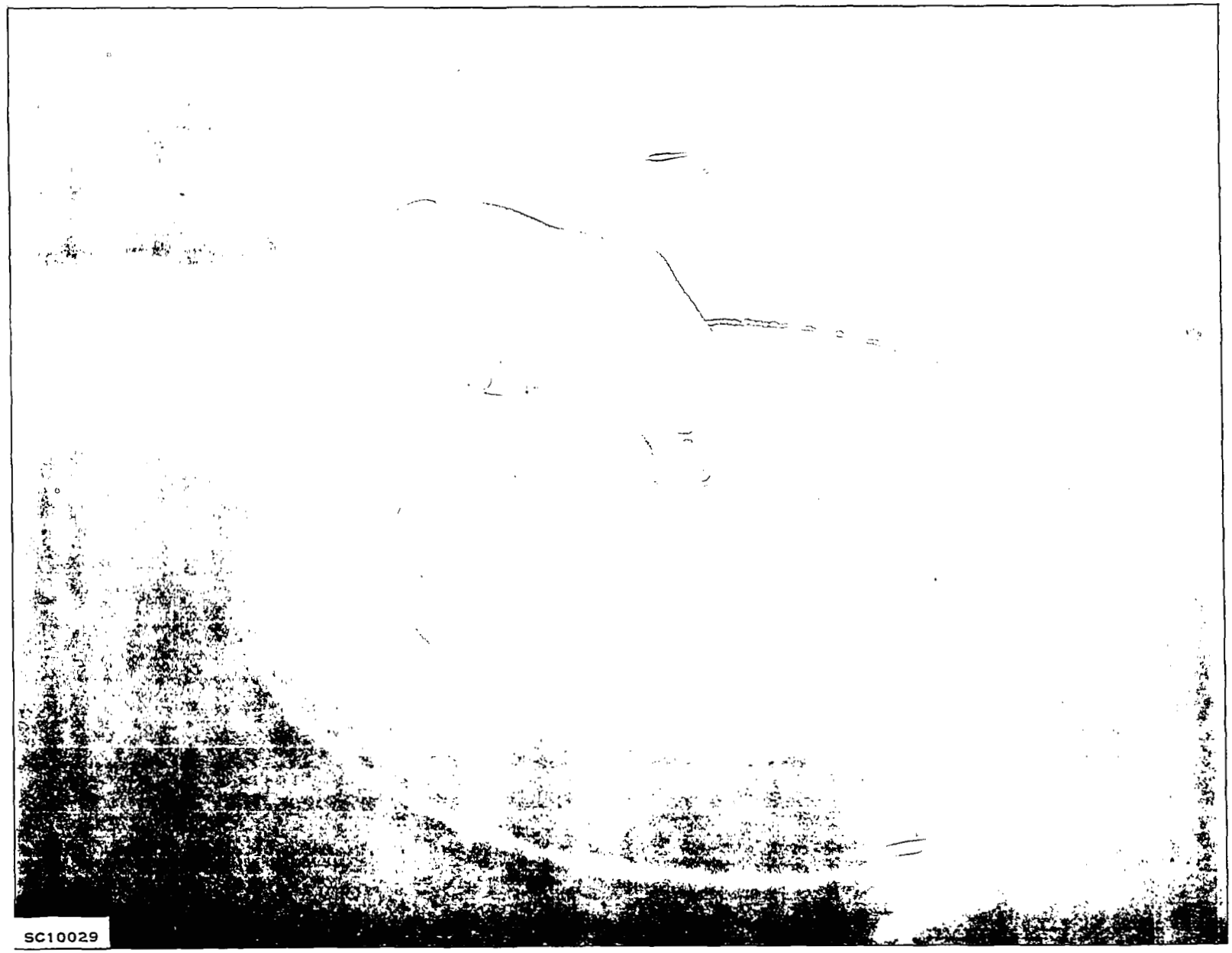

Figure 3-122. Sample Holder Properly Oriented on Fine Polisher

Depending upon the rough polishing procedure, it may be desirable to start the fine polishing with 5-μm alumina rather than the 15-μm chromium oxide. When the finer compounds are being used, it will be necessary to progressively reduce the polishing time and the pressure. It is usual to polish with the 0.05-μm alumina for less than a minute with light hand pressure to produce a flawless surface. An important step in maintaining the fine surface produced in polishing is the careful removal of the polishing residue from the sample surface. This is done most effectively with a cotton swab. The swab should first be held in a stream of clean, filtered, deionized water to soften the fibers. The sample is then held in a stream of deionized water and swabbed gently until clean. The surface can then be dried by carefully blowing it with clean, filtered air.

The decreasing size of the active surface of the semiconductor and the control required to measure diffused junction depths to millionths of an inch have made perpendicular sectioning almost obsolete as a method of evaluation. Difficult problems arise now in mounting and sectioning chips that are 0.040 inch square or less and have base widths of 20 microinches. Angle (taper) sectioning has been resorted to as a solution to these problems. For instance, a 5°-43' angle microsection produces an effective magnification of 10X. The maintenance of an exact angle is not as important as keeping the section flat across the sample surface. This is necessary for an accurate determination of the geometry of the sample.

G. MATERIALS AND TECHNIQUES FOR JUNCTION DELINEATION IN SILICON

1. General

In much of semiconductor failure analysis work, it becomes necessary to delineate the junctions on the polished silicon sample. The treatment procedure is to place an aqueous staining solution (commonly referred to as an etch or stain) in contact with the polished surface containing the junction. The solution functions by making silicon dioxide (SiO_2) soluble; in the presence of the solution, silicon monoxide, SiO, is relatively insoluble. The solution includes an oxidizing agent which stains by selectively forming over the silicon surface a layer of silicon monoxide.

The silicon monoxide forms mainly on the P-type material, giving it a darker appearance than the N-type material. This makes the demarcation between the two types of material clearly visible. It should be remembered that the P-N junction will appear as a contour. This is due to the fact that the higher concentration in P-type material will be more darkly colored. In some of the stains with higher total acid content, the N-type regions are more darkly colored, the lower the concentration. Thus, it can be seen that concentration gradients show up as a difference in shading.

Evidence indicates that the staining process in the P-type material involves an electrochemical oxidation and reduction reaction which proceeds more quickly in P-type material because of its greater free energy of reaction. In this type reaction, the electrons given up by the P-type material must be balanced out by the flow of holes from the

N-type material. Since this is in the high-resistance direction for the junction, surface leakage is the only path in which the current may flow. Also, surface leakage is enhanced by the mechanical polishing techniques previously described. This forms the basis for the most successful method of junction delineation.

2. Materials

Common silicon stains and their compositions are as follows:

1) Dash Etch:

- 3 parts by volume HNO_3 (Nitric Acid, 70 percent)
- 1 part by volume HF (Hydrofluoric Acid, 49 percent)
- 12 parts by volume HAc (Acetic Acid, Glacial, 99.7 percent)

2) 3-1 Stain:

- 3 parts by volume HNO_3 (Nitric Acid, 70 percent)
- 1 part by volume HF (Hydrofluoric Acid, 49 percent)
- 10 parts by volume HAc (Acetic Acid, Glacial, 99.7 percent)

3) 10-1 Stain:

- 10 parts by volume HNO_3 (Nitric Acid, 70 percent)
- 1 part by volume HF (Hydrofluoric Acid, 49 percent)
- 7 parts by volume HAc (Acetic Acid, Glacial, 99.7 percent)

4) 20-1 Stain:

- 20 parts by volume HNO_3 (Nitric Acid, 70 percent)
- 1 part by volume HF (Hydrofluoric Acid, 49 percent)

5) 3-1 Stain with $CuSO_4$ Solution. The $CuSO_4$ solution consists of the following:

- 10 ml of HF (Hydrofluoric Acid, 49 percent)
- 200 g of $CuSO_4$
- 1 liter of deionized water
- Add 4-to-6 drops of $CuSO_4$ solution to 10 ml of the 3-1 stain solution.

3. Techniques

The techniques for using each of the previously listed stains are as follows:

1) Dash etch. A drop of the solution is applied to the sample, which is then exposed to a strong microscope light for a period of time varying from 1 to 20 seconds. Very heavily doped regions will become visible after several seconds, and as time progresses, the more lightly doped regions will appear. On epitaxial devices, usually the color of the heavily doped substrate will range from brown to blue after 10-to-15 seconds. This etch does not accentuate crystal flaws or defects due to polishing.

2) 3-1 Stain. Within 4-to-5 seconds after a drop of the solution has been applied to the sample, the junctions will appear. Lightly doped regions can be brought out by using a light to speed up the reaction. Normally, this stain will—if used for an extended period of time—define all the junctions in a silicon wafer.

3) 10-1 stain. A drop of stain is placed on the sample and is immediately washed off as quickly as possible (within less than 1 second). This stain produces a fine line P-N junction but also greatly accentuates crystal damage or damages due to microsectioning.

4) 20-1 stain. This stain delineates the emitter, collector and vapor-growth junctions in silicon devices. For best results, a cotton swab saturated with the staining solution should be rubbed against the polished surface. Within 0.5-to-1 second after application of the stain, all junctions should appear. Because defects are emphasized by this stain, the prepared surface must be scratch free when viewed under 100X vertical illumination, if reproducible results are to be obtained.

A semiconductor surface is attacked by the stain at a rate which is dependent upon impurity type and concentration, crystallographic orientation and residual stresses produced either by polishing or during the fabrication of the device. This solution will attack an N-type material at a faster rate than it will the corresponding P-type material. The emitter and collector junctions will appear as abrupt changes in the height of the surface. These steps are the junction positions and changes in the impurity gradient.

5) 3-1 stain with $CuSO_4$ solution. This stain can be used in place of the 3-1 stain if the sample begins to show excessive staining burns (excessive material removal) before all of the junctions have been defined. Junction definition is enhanced by the deposition of metallic copper. Except for longer staining times, this stain is used in the same way as the standard 3-1 solution.

H. REFERENCES

1. The AB Metal Digest, Vol. 11, No. 2, "Polishing the Micro Section, Part 1" (Evanston, Illinois: Buehler, Ltd., and Adolph I. Buehler, Inc., 1956), pp. 4-6.

2. Ibid.

SECTION VI

THE THERMAL SCANNER

A. GENERAL

The thermal scanner or infrared microradiometer (Figure 3-123) measures the intensity of infrared radiation emitted from a heated object. The output of the thermal scanner can be related to a definite temperature by means of a calibration curve, provided the surface of the object has a uniform emissivity. To insure this uniform emissivity, the surface of the object is sprayed with a thin coat of flat black paint.

Infrared radiation is collected from the subject area on the surface of the object by a reflecting microscope type objective. This subject spot varies from 0.001 inch to 0.0004 inch in diameter, depending on the power of the objective. The objective then focuses the radiation on an indium-antimonide photovoltaic infrared detector which is maintained at the temperature of liquid nitrogen. The detector is kept biased to zero volts for maximum sensitivity and optimum signal-to-noise ratio. As the intensity of the incident radiation increases, the voltage across the detector rises exponentially. Since this signal is in the low microvolt range, it is necessary to amplify it considerably. In order to simplify the amplification, an ac signal is obtained by placing a mechanical chopper between the objective and the detector. The signal is chopped at a frequency of 900 Hz. The chopper also provides a reference signal by means of a photo diode and a light source, which is used to demodulate the infrared signal after it is amplified.

In order to properly align and focus on the heated object, it is necessary that a given point on the object be coincident on the detector and on the focusing screen. This is done by an eyepiece and mirror which can be moved into place between the detector and the objective. Light is also supplied along the same optical path by means of a vertical illuminator. When the instrument is scanning a subject, the mirror is moved aside to reduce the signal attenuation to a minimum. This improves the repeatability of the instrument as well.

The object to be scanned is mounted in an appropriate holder which will allow it to be properly powered. The holder is then mounted on the substage of the thermal scanner, which also functions as the focusing mechanism. The stage can be driven continuously in the x-direction up to 0.270 inch and can be stepped in the y-direction in increments from 0.002 inch to 0.0001 inch.

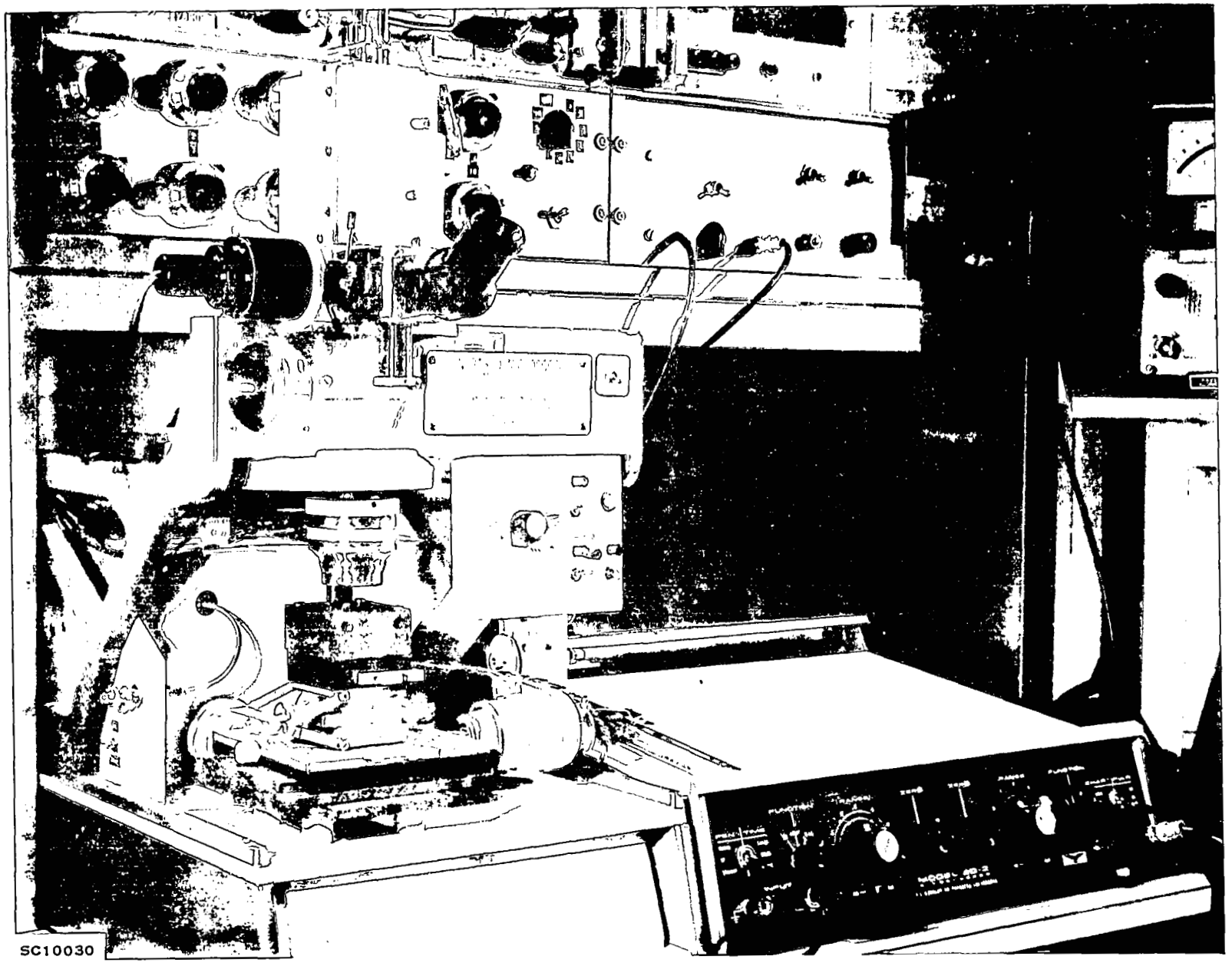

Figure 3-123. Thermal Scanner

B. CAPABILITIES AND LIMITATIONS

In general, the thermal scanner is used to measure surface temperatures on the microscopic level without making physical contact with the surface. Any device of reasonable size and shape with a flat surface, which can be heated or dissipates power can be scanned by the thermal scanner. The main limitation of size is the fixed distance from the stage at its lowest position to the focal plane of the objective. This distance ranges from 1.5 inches to 2.0 inches, depending upon the objective in use.

The thermal scanner can detect thermal gradients of 0.5°C at 60°C with relative ease and can measure absolute temperature with an accuracy of $\pm$ 1.0°C at 60°C. The thermal scanner has a geometrical resolution of down to 0.0002 inch with the 52X objective.

There are three types of data which can be obtained with the thermal scanner. The first and most rapidly obtainable data is a single profile or several profiles taken along some point of interest such as along an emitter finger or across several fingers in a transistor. A more complex form of data is the thermal contour map in which isotherms are drawn on an enlargement of the surface geometry of the device. This requires a series of scans to be taken across the entire device at given increments. The third form of data is the thermal rise and fall times of a device. This is the time required for the device to heat up to a given temperature and to cool off to room temperature. The only limitation is that this time constant be longer than the rise and fall time of the electronics of the scanner (about 10 ms).

C. INTERPRETATION OF DATA

Three factors are considered when interpreting data from the microradiometer; these factors are:

1) The effect on temperature distribution, resulting from removal of the can from the device.

2) The change in the heat dissipation characteristic of the device due to the presence of paint on the wafer.

3) The thermal properties of the materials used in the device, i.e., Si, Ge, Au, Al, etc.

In interpreting data from an instrument, accuracy must be borne in mind at all times. This is especially important with the infrared microradiometer.

Consider the first data factor: the effect of removing the device's can. With the can removed, the thermal mass of the unit is reduced. The lower thermal mass

will allow more rapid changes in temperature on the unit. The reduced surface area for heat dissipation allows the unit to rise to a higher temperature for a given amount of power dissipation. Without the can, the wafer's ambient is no longer a trapped gas; instead, cooling by convection currents takes place. Therefore, it can be assumed that the unit would be cooler at a given power dissipation due to the direct convection cooling. However, at temperatures near the room ambient the convection currents would have only a slight effect.

With respect to the second data factor, some studies have been made on large wafers used as the active element in power transistors, to determine the consequences of paint on the wafer. The paint had no appreciable effect on the absolute temperature or on the temperature distribution if the thickness of the paint was less than 0.003 inch. The paint acted as a shield for the wafer, similar in effect to the shielding presented by the can. This reduced the effect of direct convection at higher temperatures. As an outcome of this study, it was found that a painted, decanned device acts very much like a canned device with respect to wafer temperature both at high- and near-room temperature.

The key to interpreting data from the infrared microradiometer is an understanding of the third data factor, the thermal properties of the materials used in the devices, such as gold and silicon. Metals in the pure form, such as gold and aluminum, are relatively good heat conductors. Whenever a hot spot occurs in the vicinity of an evaporated lead or a contact area, the good thermal conductivity of the metal causes spreading of the thermal gradient over a relatively large area. The same phenomena is observed in semiconductor materials since they cannot support large temperature gradients within a small area. Briefly, extremely small, isolated hot spots have not been detected with the microradiometer. For this reason, it is doubtful that they exist in a monolithic microcircuit.

SECTION VII

OTHER ANALYSIS TECHNIQUES

A. ELECTRON MICROSCOPY

1. General

Electron microscopy has two definite applications in failure analysis:

- Extension of the range of physical inspection.
- Chemical analysis of small particles.

2. Physical Inspection

The lower limit of resolution of any physical inspection system is determined by the wavelength of the radiation utilized to illuminate the specimen being examined. The Rayleigh [1/] limit of resolution can be expressed as:

$$Z = 0.61 \cdot \frac{\frac{\lambda_o}{n}}{\sin u} \tag{30}$$

where

λ_o = wavelength of electron in vacuum.

n = index of refraction

sin u = ratio of the effective lens radius to the square root of the sum of the squares of the effective lens radius and the object-to-lens distance.

For an electrostatic lens system, the lower resolution limit can be expressed in terms of the accelerating potential. An electron's wavelength is related to its momentum by the De Broglie law:

$$p = \frac{h}{\lambda} \tag{31}$$

where

p = momentum

h = Planck's constant

λ = wavelength of electron

If the velocity v of the electron was acquired by accelerating through a potential difference, V, then

$$\frac{mv^2}{2} = eV \tag{32}$$

$$v = \sqrt{\frac{2eV}{m}}$$

where

m = mass

e = charge on electron

or

$$p = m\sqrt{\frac{2eV}{m}} = \sqrt{2meV} = \frac{h}{\lambda}$$

or

$$p = \frac{h}{\sqrt{2meV}} \tag{33}$$

where

h = Planck's constant = 6.62×10^{-34} J- s

m = mass of an electron = 9.11×10^{-31} kg

e = charge on electron = 1.602×10^{-19} C

therefore

$$\lambda = \frac{12.24 \times 10^{-8}}{\sqrt{V}} \text{ cm} \tag{34}$$

or

$$Z = \frac{7.47}{\sqrt{V} \cdot \sin u} \tag{35}$$

Hence even with moderate accelerating potentials, the wavelengths of electrons are within an order of magnitude of those of X-rays, or about 1/1000th of the wavelengths of visible light.

Specimen preparation techniques for physical inspection usually are variations of the two general techniques:

- Preparation for direct transmission.
- Preparation for replica inspection.

Direct transmission allows inspection of the specimen directly. The specimen must be thin enough to transmit electrons without excessive scatter (usually of the order of a few hundred angstroms). Specimens are etched or lapped to the proper thickness.

Replica inspection involves making copies of the surface and using these as specimens. The detailed instructions for replica preparation can be found in the literature. In general terms the procedure involves the following steps:

- The surface to be studied is coated with a plastic material (usually nitrocellulose).
- The plastic is dried in place and then peeled away from the surface.
- The plastic is then placed on a specimen grid.
- A thin layer of carbon is sputtered over the plastic surface.
- This layer of carbon is then shadowed with platinum (this causes highlighting of the relief features).
- The plastic material is dissolved, leaving a thin carbon film. (This is usually done with amyl acetate.)

When the preceding steps have been completed, the replica is ready for viewing.

For an example of physical inspection made possible by electron microscopy, consider Figures 3-124, 3-125 and 3-126. These illustrations were taken from a metallization study. The initial condition of an aluminum stripe is shown in Figure 124. The effects of high-current density ($> 1.0 \times 10^6$ amperes/cm^2) and high temperatures (~150° C) are shown in Figure 3-125. Note the conglomeration of metal into regions of enhanced thickness. The effects of high temperature gradients and chemical corrosion of thin aluminum stripes are shown in Figure 3-126, which typifies stress corrosion of thin (~30-to-70 microinches) stripes of aluminum over silicon dioxide.

3. Chemical Analysis of Small Particles

a. General

One of the more troublesome problems of failure analysis is the identification of small particles in regard to their chemical content. Electron diffraction techniques are now being utilized to perform these analyses.

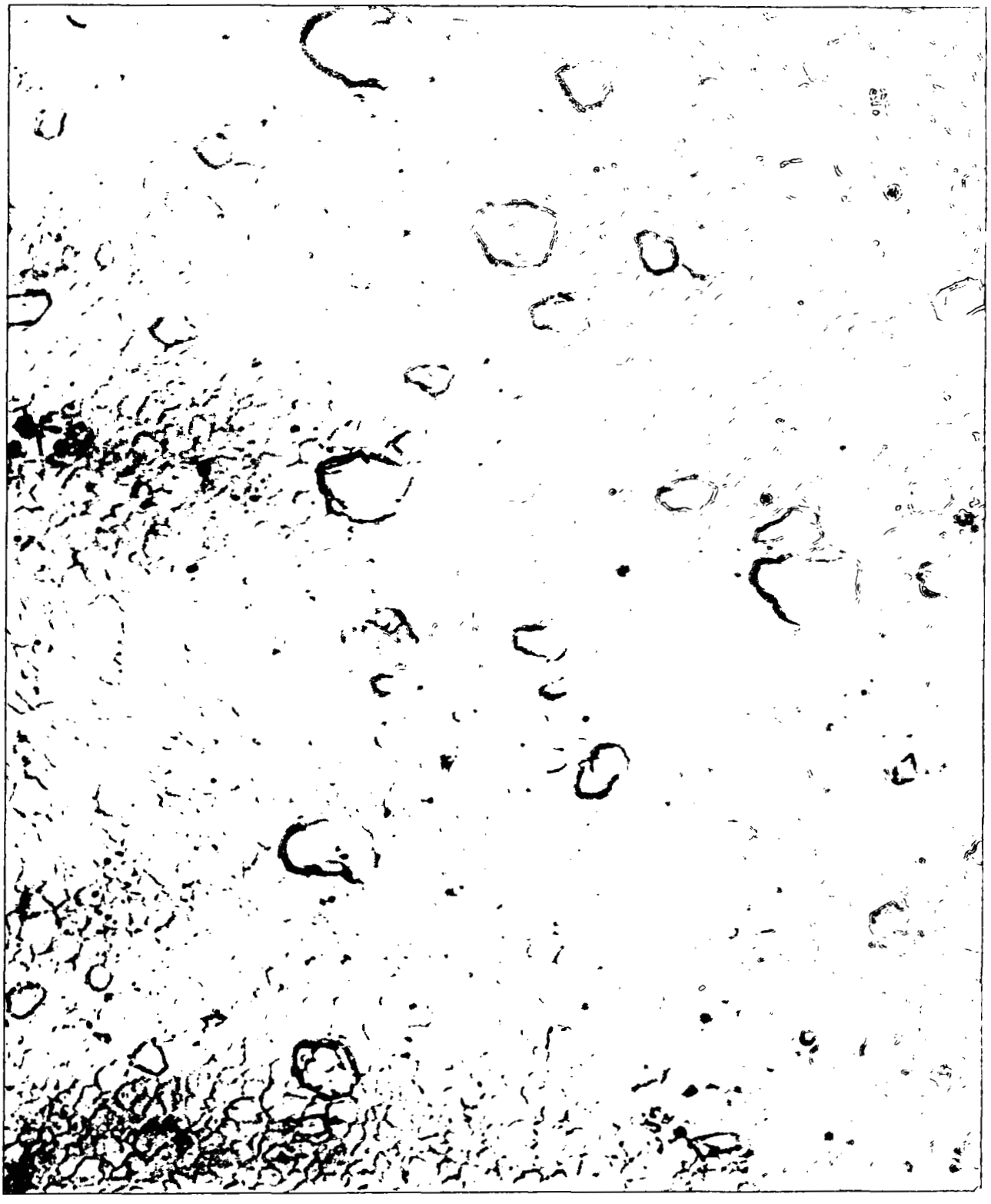

Figure 3-124. Electron Micrograph of Aluminum Stripe before Stressing

Figure 3-125. Electron Micrograph of Aluminum Stripe After Subjection to High-Current Density and High Temperature

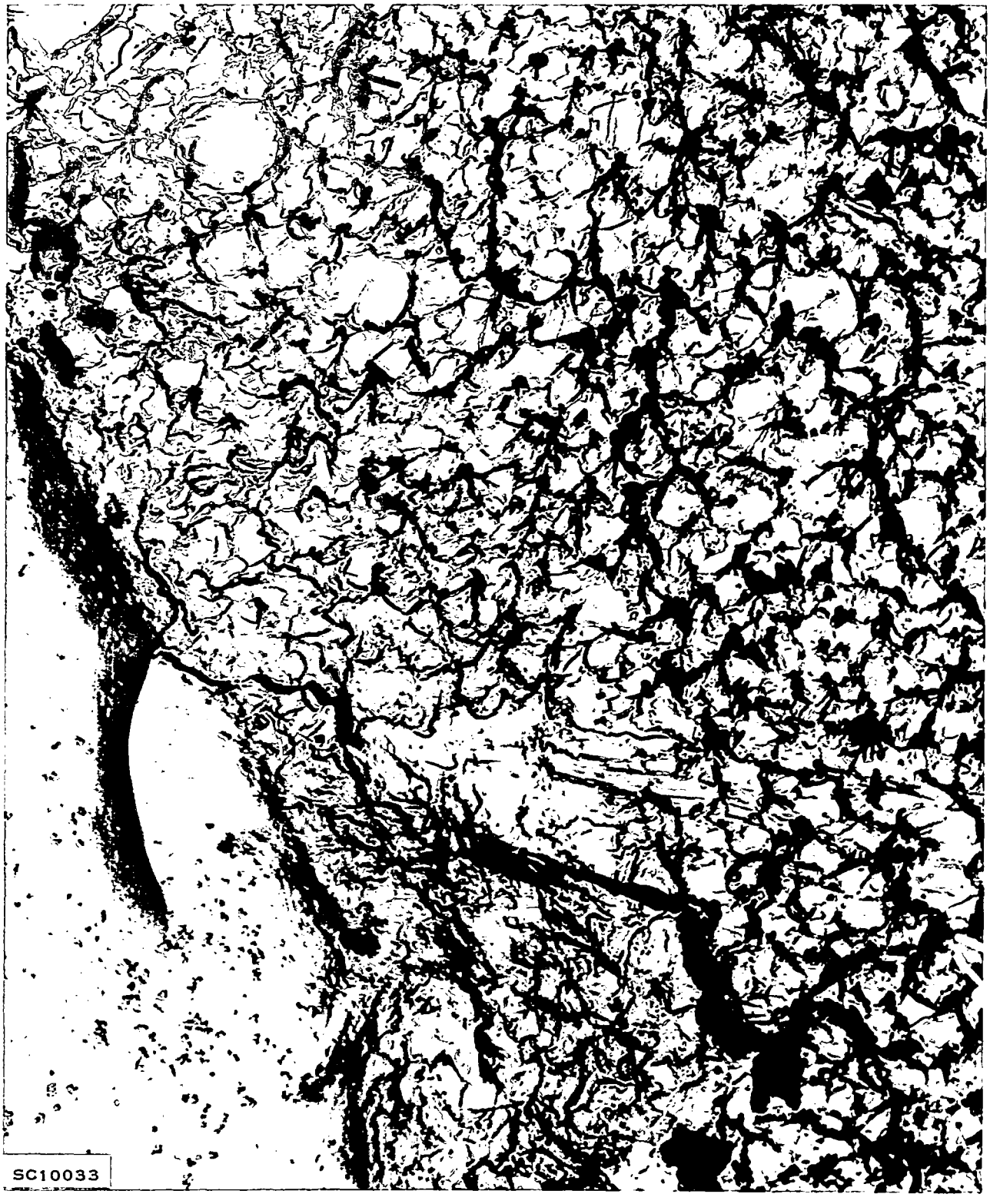

Figure 3-126. Electron Micrograph of Aluminum Stripe After Subjection to High-Temperature Gradients and Chemical Corrosion

b. Electron Diffraction

Bragg reflection[2] is an important and characteristic feature of wave propagation in periodic structures. Bragg reflection occurs also for electron waves in crystals. The observations of Davisson and Germer[3] on the wave nature of the electron were observations of the Bragg reflection of an electron beam from the crystal surface.

W. L. Bragg found that one could account for the position of the diffracted beams produced by a crystal in an X-ray beam by a simple model which assumes that X-rays are reflected specularly from the various planes of atoms in the crystal. The diffracted beams are found only for special situations in which the reflections from parallel planes of atoms interfere constructively.

Consider in the crystal a series of atomic planes which are considered to be partly reflecting for radiation of wavelength λ, and which are spaced equal distances d apart, as in Figure 3-127. The path difference for rays reflected from adjacent planes is $2d \sin \theta$. Reinforcement of the radiation reflected from successive planes will occur when the path difference is an integral number n of wavelengths. The condition for constructive reflection is:

$$2d \sin \theta = n\lambda \tag{36}$$

where

θ = angle of incidence

This is the Bragg law.

c. Application of Electron Diffraction

The illustration shown in Figure 3-128 is a typical diffraction pattern produced by passing an electron beam through a small sample. This particular pattern was produced by an aluminum standard. By utilizing a standard whose plane spacings are accurately known, one can calibrate subsequent patterns. Consider the Bragg law:

$$n\lambda = 2d \sin \theta \tag{36}$$

The terms to the left are dependent only upon the electron beam energy. The terms to the right are dependent upon the sample. Thus one can write:

$$2d_{Al} \frac{X_{Al}}{y^2 + X_{Al}^2} = 2d_{un} \frac{X_{un}}{y^2 + X_{un}^2} \tag{37}$$

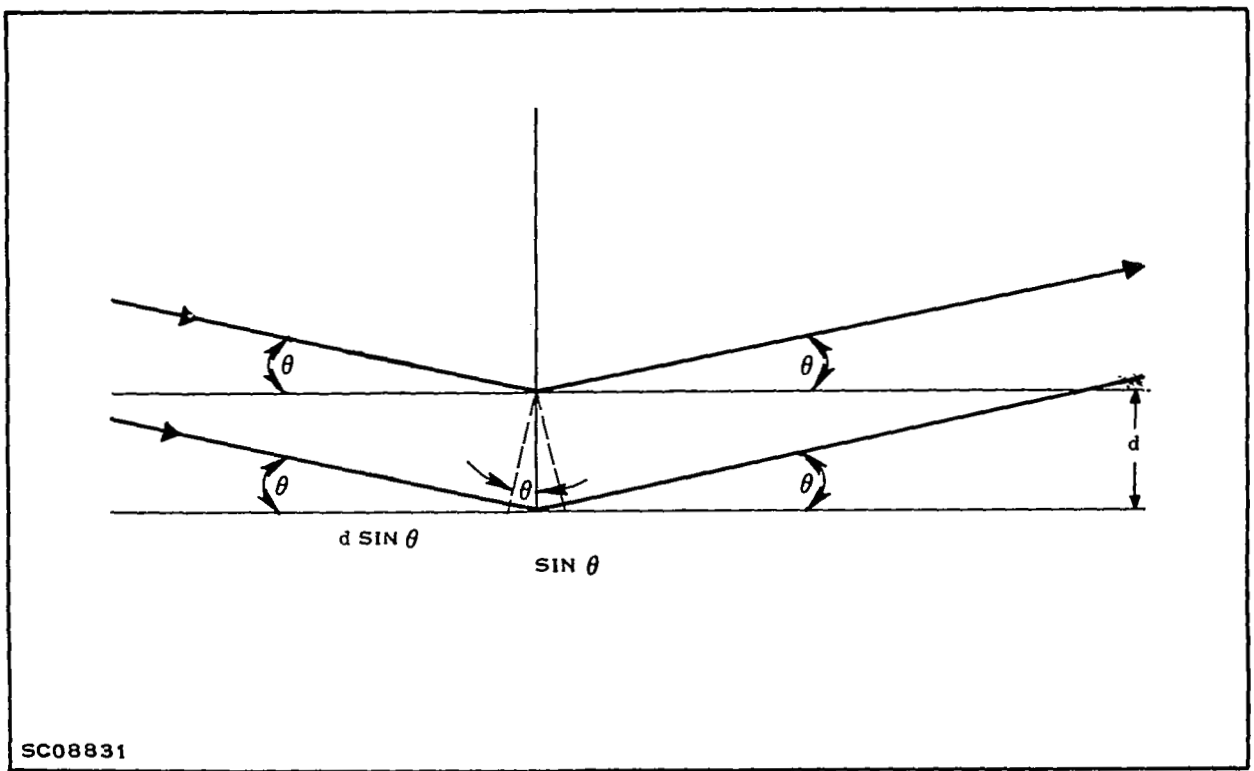

Figure 3-127. Model of Crystal Planes, an Illustration of Electron Diffraction Effect

where

X_{Al} = Spacing of rings on film used during aluminum diffraction

X_{un} = Spacing of rings on film used during unknown diffraction

un = Unknown

y = Specimen-to-film plane spacing

d_{Al} = Atomic plane spacing in Al sample

d_{un} = Atomic plane spacing in Al unknown sample

Since

$$y \gg X_{Al} \text{ and } y \gg X_{un}$$

or

$$d_{Al} X_{Al} = d_{un} X_{un}$$

then

$$d_{un} = \frac{X_{Al}}{X_{un}} \cdot d_{Al}$$

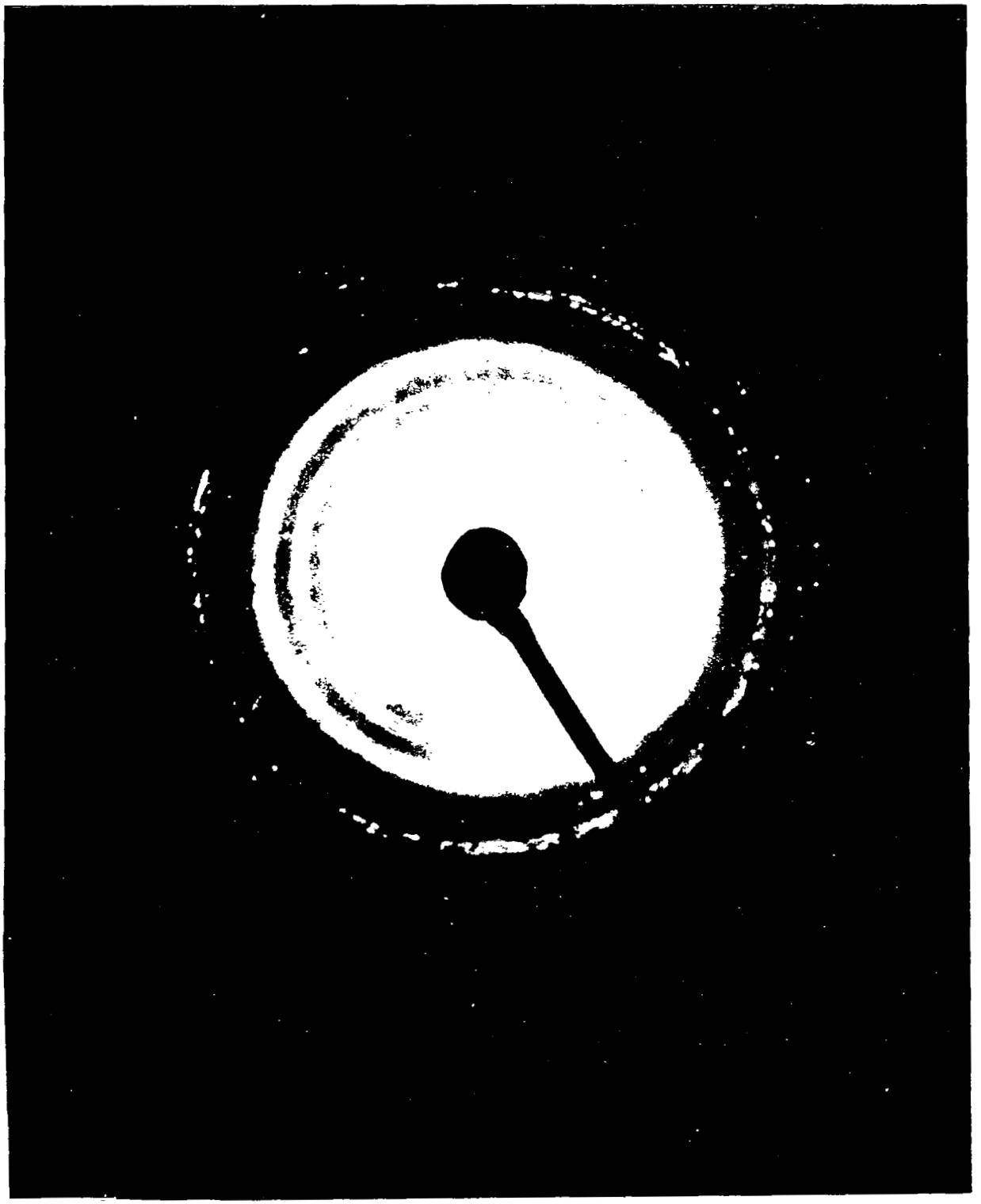

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Figure 3-128. Electron Diffraction Pattern of Aluminum

Hence

$$d_{un} = \frac{K}{X_{un}} \tag{38}$$

where

$$K = \text{constant} = X_{Al}\, d_{Al}$$

A photomicrograph of an irregularly shaped growth from the metallization stripe of the subject is shown in Figure 3-129. The subject was replicated by the electron micrographic techniques previously described. The electron micrograph and the electron diffraction pattern obtained from this subject are shown in Figure 3-130. It was necessary to ensure that the crystalline structure under study was actually adhering to the replica. This was done by making a photomicrograph of the subject before and then after the replica was completed and stripped. This replica was placed in the electron microscope, and the crystal was located on the replica by use of the visual viewing screen. See Figure 3-131.

After orienting the replica properly, the electron microscope was placed in the diffraction mode (150 kV diffraction) and the pattern was obtained as illustrated in the upper right hand corner of Figure 3-130. By comparing the unknown pattern with the pattern of known elements as indicated in the ASTM X-ray powder pattern file,[4] the unknown element or compound was identified. The standard selected for this comparison was molybdenum nitride (Mo_2 N). In the following tabulation, which is a comparison between the atomic-plane spacing ratio of the standard and that observed in the replica, it should be noted that the unknown compound is most certainly molybdenum nitride, due to its close agreement with the standard:

Standard	Observed
2.410	2.40
2.088	2.09
1.476	1.47
1.259	1.24
1.206	1.20
1.0441	1.04
0.9582	0.953
0.9338	0.930
0.8527	0.855
0.8040	0.800

The application of electron microscopy to failure analysis is in the early stages of development. As new techniques are perfected, this most useful tool will burgeon into an invaluable asset to the failure analyst.

Figure 3-129. Electron Micrograph of Irregular Growth on Stripe of Device

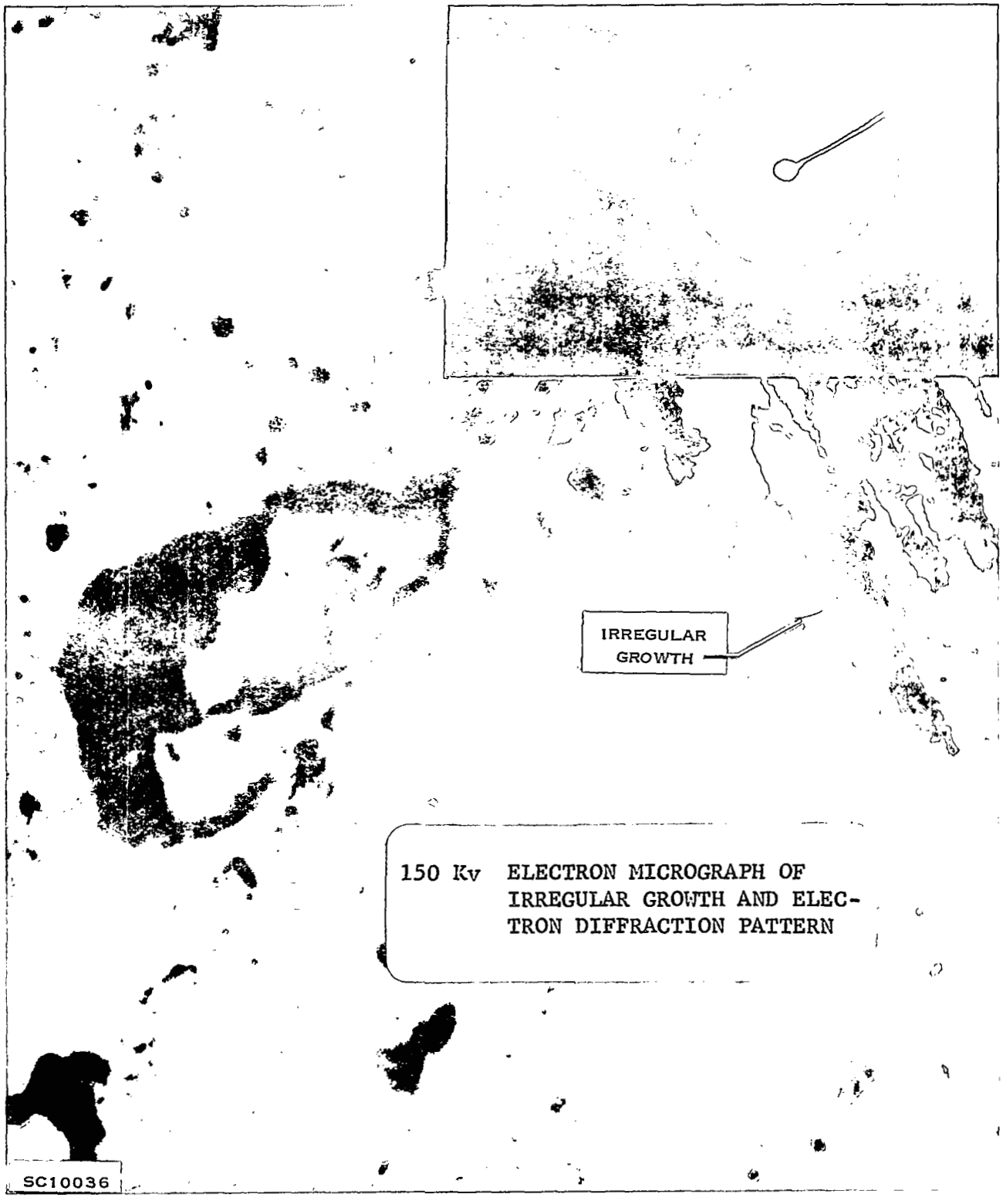

Figure 3-130. Electron Micrograph of Irregular Growth and Electron Diffraction Pattern

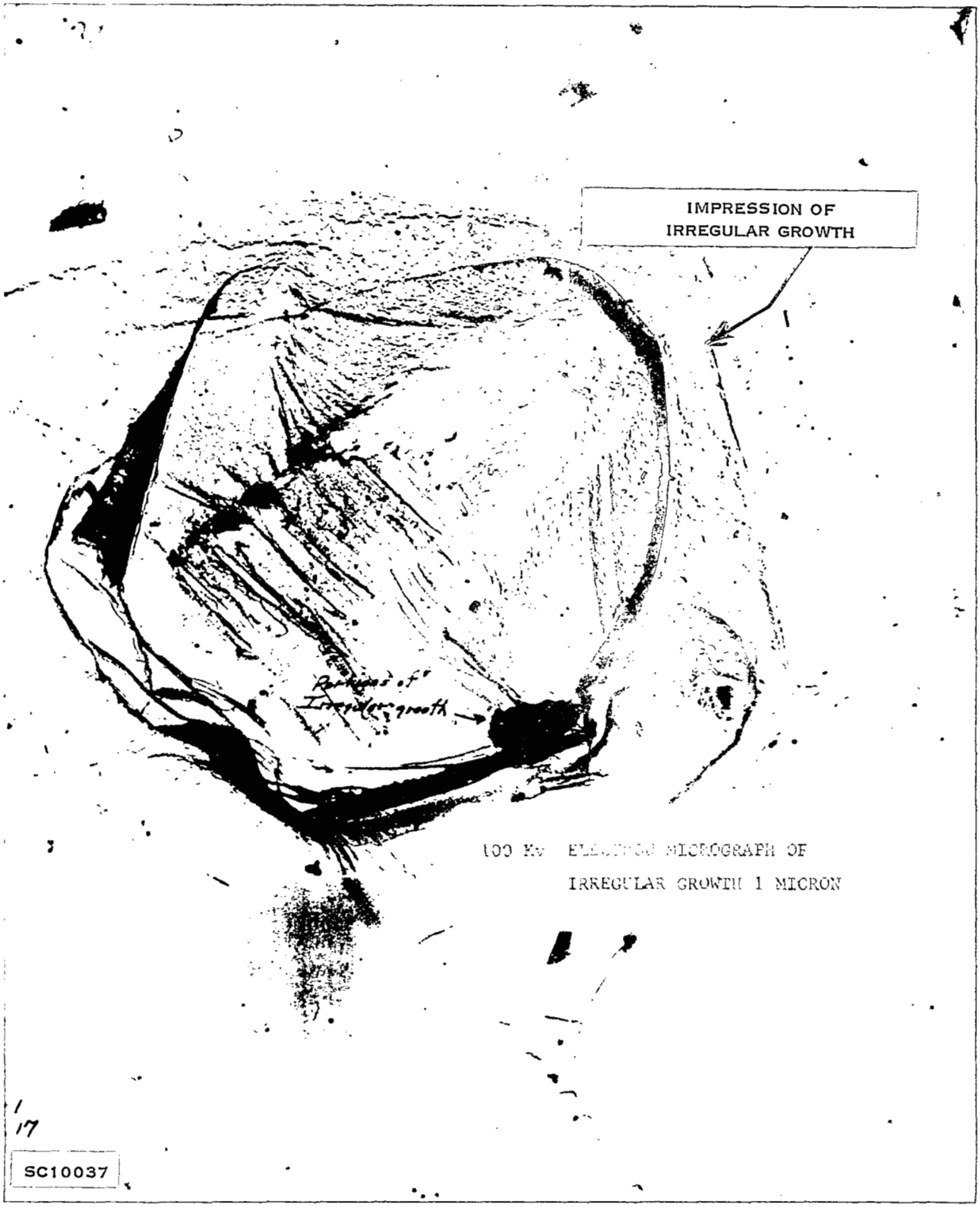

Figure 3-131. Electron Micrograph of Irregular Growth

B. ELECTRON MICROPROBE

1. General

The electron microprobe is used to obtain a chemical-element analysis of a microscopic area. The analysis of an area of interest is performed in the following manner:

1) Areas of interest are identified by means of a microscope.

2) An electron beam directed to an area that is to be analyzed, produces X-rays due to the electron bombardment.

3) The X-ray wavelengths are separated by an analyzing-crystal (each chemical element produces its own characteristic X-ray spectrum).

4) The now-separated X-rays are detected by flow-proportional counters, as voltage pulses.

5) The pulses are counted and read out as digital or analog data. (The pulse-count rate is proportional to the X-ray intensity and thus is proportional to elemental concentration.)

More detailed descriptions are presented in the literature.[5,6]

The digital output of an analyzing channel of the microprobe's electronics is subject to statistical deviation to the same relative degree as any other counting technique. Since the microprobe produces very large count rates, the standard deviation is actually about three times as great as would be expected from ideal statistics. For example, deviation occurs because the sensitivity of the equipment is degraded by the high background counts. And the background counts for a given element will change with relative variations in the composition of the sample. Furthermore, measurements of very low concentrations require very long counting times, which are not practical because the electron-beam current drifts. Thus, for measurements of an area of very low chemical-element concentration, pure substrate material is essential if the background count is to be at a tolerably low level. The statistical errors are evaluated for each quantitative analysis, and generally they are ± 3 percent at the 95-percent confidence level.

2. Sample Preparation

Samples must be solid and stable in a vacuum. They must have reasonably high melting points (> 100° C). Almost any standard mounting material can be used,

but nonconductive material must have a thin carbon layer applied across the surface to allow a path for discharging. If analysis for light elements (atomic numbers 5 through 13 is required, the carbon coating should be deleted, because it would absorb the emergent X-rays. As a replacement for the carbon, a coating of conductive mounting material should be applied to provide a discharge path.

If the analysis requires microsectioning of the sample, it should be metallurgically polished down to 0.25-μm polishing sizes. (Refer to Section V in this volume for a description of metallurgical sectioning of the semiconductor element.) Rounding of edges and relief of structures should be kept to a minimum since surface relief may distort the relative accuracy of the microprobe's data output.

The types of analysis that the electron microprobe performs, the time required for each type of analysis, and the limitations of the instrument are shown in Table 3-1.

3. Examples of Electron Microprobe Chemical Element Analysis

Two examples of the use of the electron microprobe to perform chemical-element analysis as an aid in determining why a monolithic microcircuit device failed will be presented here.

A photograph of a device that was undergoing failure analysis is shown in Figure 3-132. The microprobe was used to obtain a chemical-element analysis of the previously identified area of interest. A photograph of the resulting current (electron beam) display is shown in Figure 3-133. From this analyst it was determined that the area had been contaminated by a compound of chlorine. The qualitative electronic display shown in Figure 3-134 reveals the extent of the surface distribution of the chlorine contaminant. No other heavy elements were found. The device was not tested for the possible presence of "light" elements. Examination of the microprobe test data and the device led to the conclusion that a compound of chlorine had entered the device through a leak in the package and had caused a galvanic reaction that resulted in device failure.

The second example of meaningful results that may be obtained from a microprobe study is shown in Figure 3-135. The photograph shows the location of a particle of foreign material that previously had been identified as the cause of the device's failure. When the microprobe was used to analyze the area containing the foreign particle, the foreign material was found to have a high copper content. The surface distribution of the copper is shown in Figure 3-136.

Table 3-I. Chemical-Element Analytical Capabilities of the Electron Probe Microanalyzer

Type of Analysis to Be Performed	Surface of Area Being Analyzed		Conditions Required for Data Readout			
	Range-of-Size of Area (μm)	Limitations Imposed by Equipment	Element to be Detected		Minimum Detectable Concentration (ppm)	Approximate Counting Time Required for Detection (Hours)
			General Classification	Atomic-Number Range		
Qualitative analysis of area being investigated	0.1 to 200.0	Useful data input arises only from surrounding material and material less than 2 μm beneath surface	Heavy elements	13 to 90	> 500	2 to 3
			Lighter elements	11 to 12	> 1,000	1
			Lightest elements	5 to 10	> 10,000	4
Quick homogeneity check	1.0 to 200.0 Various areas of surface are randomly sampled	If very low concentrations are analyzed, background counts must be taken from a pure substrate	Heavy elements	13 to 90	> 1,000	1
					> 500	2
					> 100	6 to 8
Quantitative analysis of area	> 5.0 (diameter) < 5.0 (depth)	Surface must be polished (0.25-μm diamond) and flat	Heavy elements	13 to 90	> 1,000	2
					> 500	3
					> 100	8
Quantitative analysis at points along a line	5.0 μm by 2 mm mechanical scan	Surface must be polished flat	Heavy elements	13 to 90	> 1,000	2 hours, plus $3\ (10)^{-3}$ hour/μm of scan
Qualitative electronic display	300 by 300	Gives electronic picture of surface, which relates to atomic number being scanned	Heavy elements	13 to 90	> 1,000	1

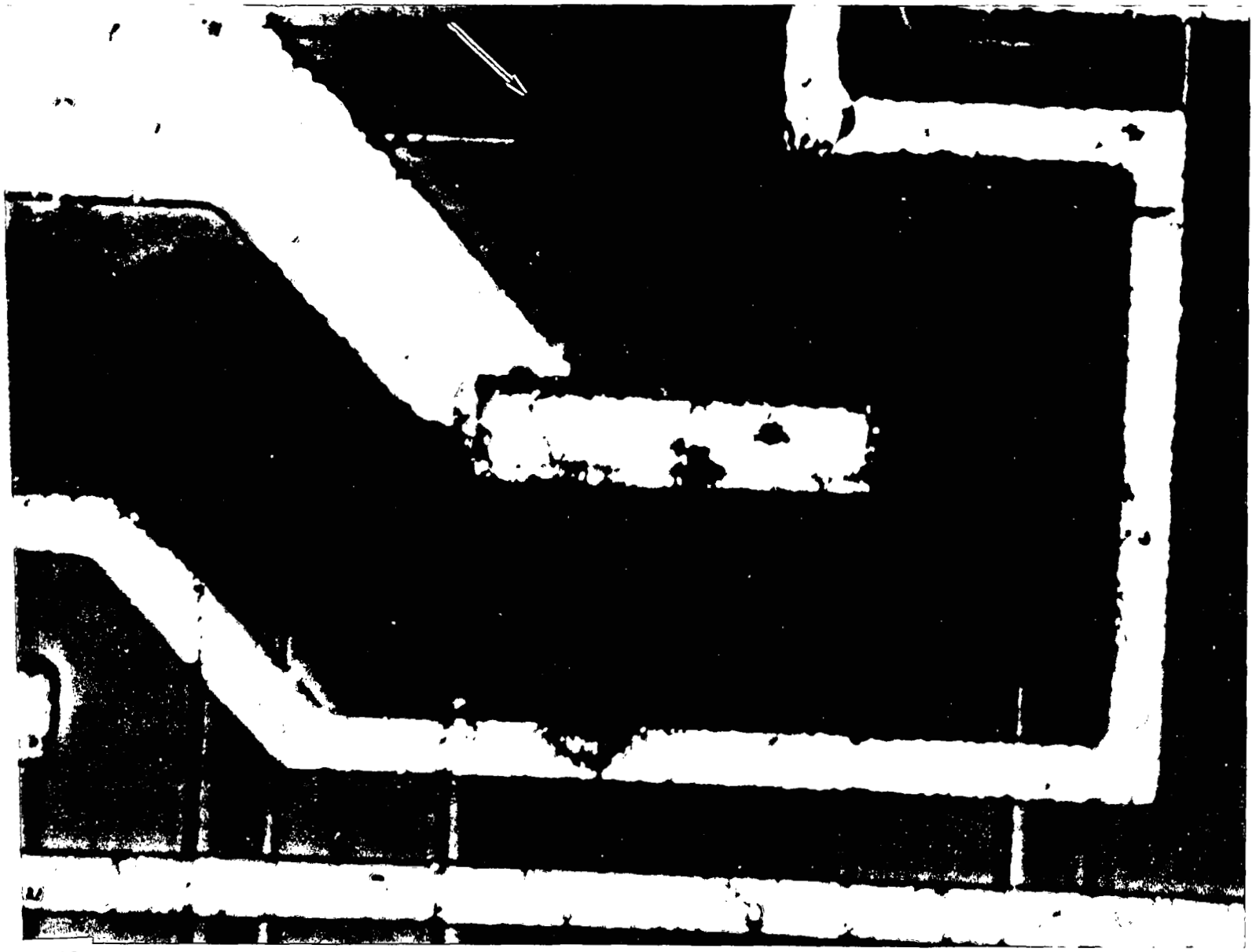

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Figure 3-132. Monolithic Microcircuit with Lead Decomposition

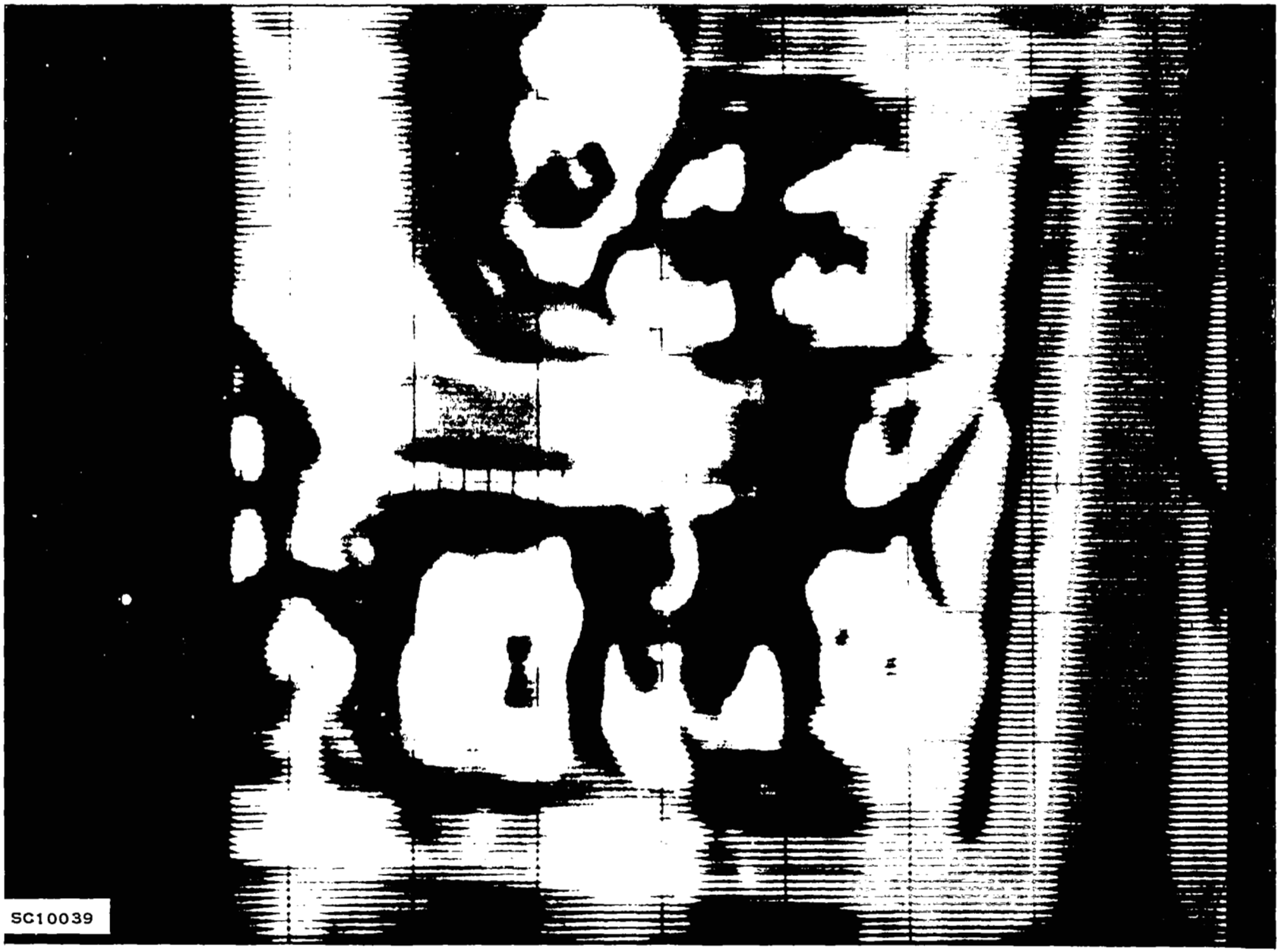

Figure 3-133. Microprobe Sample Current Display of Area with Lead Decomposition

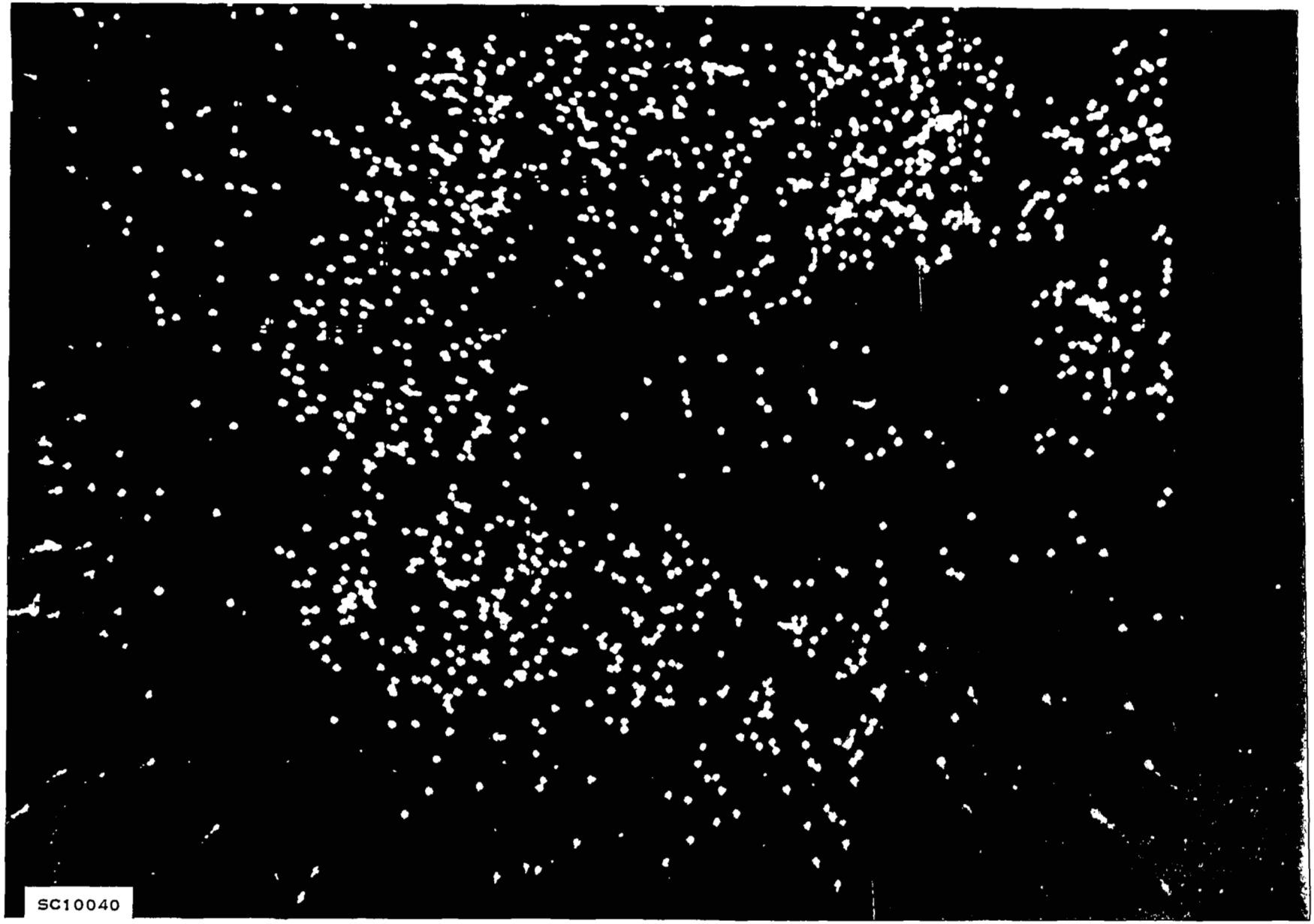

Figure 3-134. Microprobe Display of Chlorine Surface Distribution at Area with Lead Decomposition

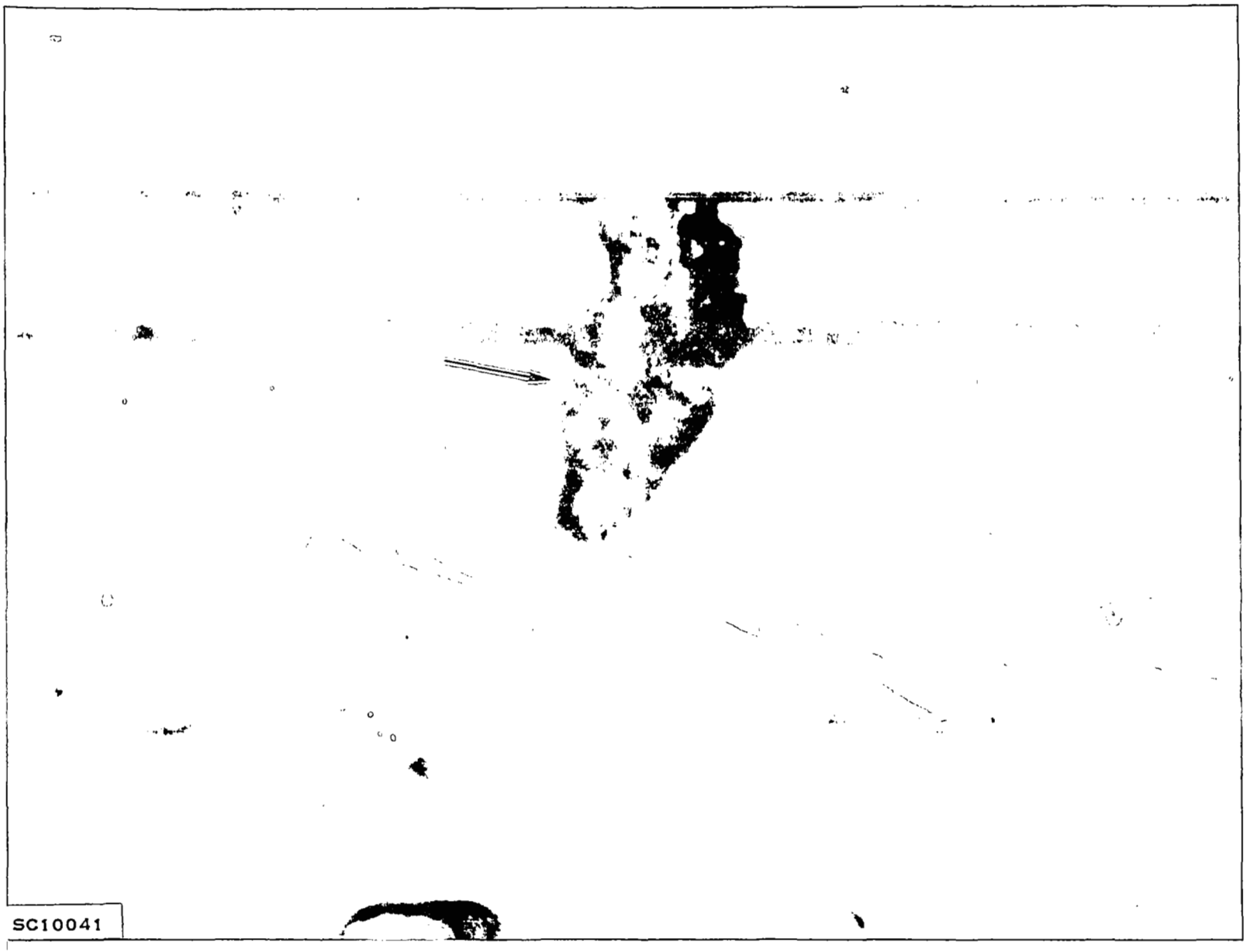

Figure 3-135. Monolithic Microcircuit with Particle of Foreign Material

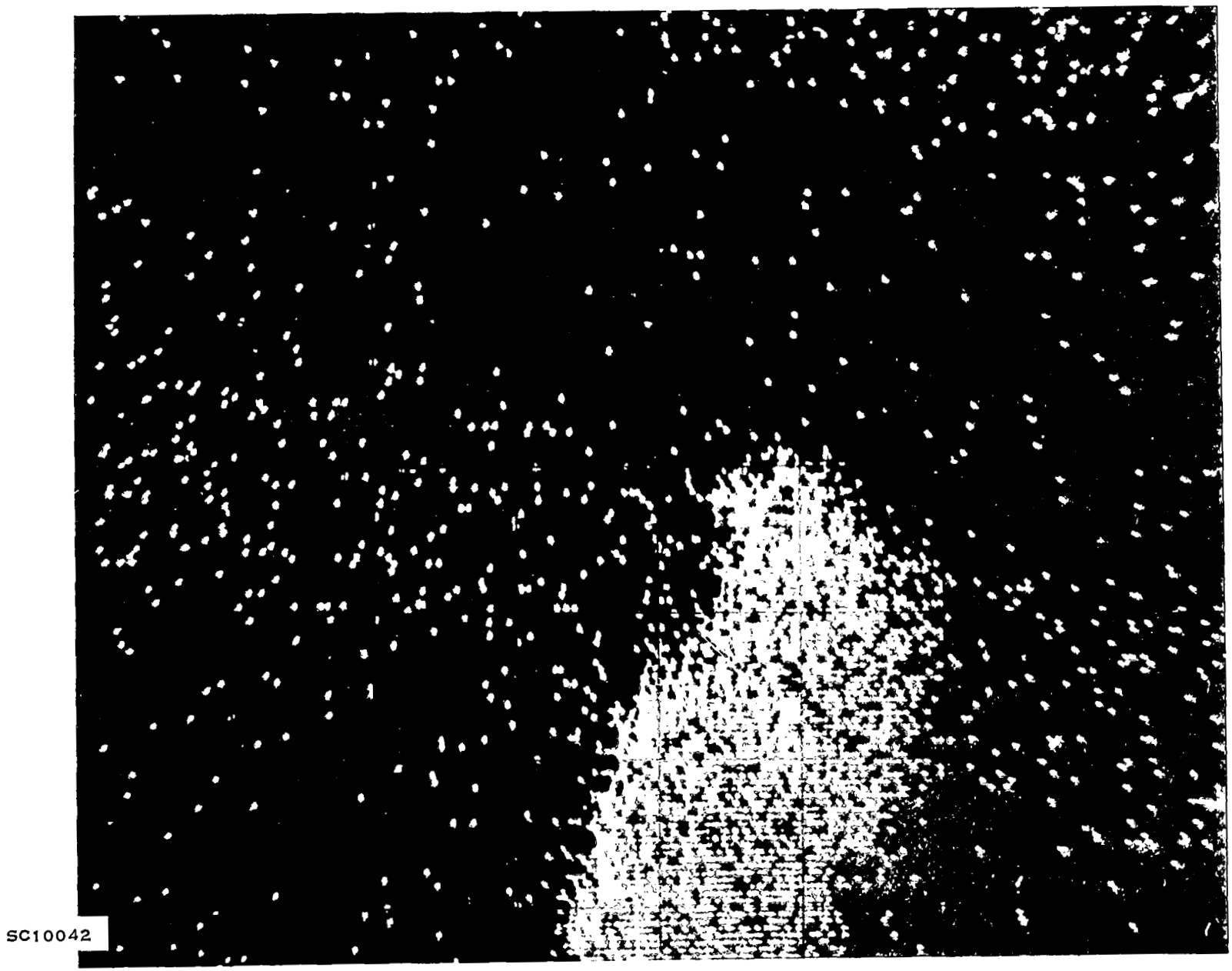

Figure 3-136. Microprobe Display of Copper Surface-Distribution at Area with Foreign Material Particle

C. REFERENCES

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